IJITCE

ISSN 2347- 3657

International Journal of Information Technology & Computer Engineering

Email : ijitce.editor@gmail.com or editor@ijitce.com

International Journal of Information Technology & Computer Engineering

ISSN 2347–3657

Volume 7, Issue 4, 2019

FRONT DESIGN AND IMPLEMENTATION OF HIGH SPEED HYBRID DUAL D-FIFO-FF (FLIP-FLOP) SYNCHRONIZER USING VERILOG

[1] Dr. A. Vinoth, [2] Dr.T. Krishnamoorthy, [3] A. Ramesh

[1] Professor, Department of ECE, AM Reddy Memorial College 0f Engineering and Technology, Andhra Pradesh 522601

[2] Associate Professor, Department of ECE, AM Reddy Memorial College 0f Engineering and Technology, Andhra Pradesh 522601

[3] Assistant Professor, Department of ECE, AM Reddy Memorial College 0f Engineering and Technology, Andhra Pradesh 522601

ABSTRACT:

Phase Measurement in certain applications where signal and its related information needs to be sustained synchronously results in to measure different phases for the application intended. Such orthodox systems would emphasize on measurements of time and phases implementing as an original mixed signal approach. This imparts uncertainty of the different phases in regards to recovered signals. To initiate such intricacies, specifically related to phase shift changes in FPGA, we impart the specific design logic core such as synchronizer and digital phase detector module for phase measurement system providing higher resolution and better precision in specific range of few Pico seconds. In this design scenario we estimate the design of the synchronizer and phase detector using Dual D-flip flops such module level modifications would arise systematic sampling over the phase detected signal. Our design with Dual D-FF would suffice the estimation of the model for customized model for Synchronizer resulting in Power and Area for respective test benchmark and has been compared and tabulated with existing system synchronizer. The design is estimated with mathematical modeling to emphasize the correct scenario for the synchronized values observed and its phase detection using Dual D flip flop. Our design methodology is implemented using Verilog HDL using HDL designer series and modelled for its netlist analysis using Xilinx Spartan 3 XCS 200TQ-144.

I. INTRODUCTION:

Postulation for the different elements in the phase measurement information has to be calibrated to establish synchronization of

ISSN 2347–3657
Volume 7, Issue 4, 2019

different digital circuits and modules. To model and implement full digital architectures and futuristic reconfigurable devices and technologies such FPGA {field programmable gate array} would preside in current era. To develop a certain design, we have to consider the runtime analysis would arise importance of latency protocols to maintain constant phase differences which are observed in recovered signals.

In FPGA circuitry, to register shift phase changes in the order of 20 -100 pico seconds a certain logic module must be available. For establishment of the constant phases we need to model and initiate the current extraction of the relative phase data where the calibration of the systems should be maintained.

In certain experiments, for example, in high vitality material science (HEP), preservation of stage connection between basic flags all through the investigation runtime is a fundamental condition. In late pattern for reduced execution of full computerized designs, reconfigurable equipment advancements, for example, field-programmable entryway exhibits (FPGAs) assume an extremely overwhelming job. Mainstream idleness basic correspondence connect benchmarks utilized in HEP examinations, for example, gigabit handset and timing-trigger and control framework over inactive optical system innovation are executed in FPGAs straightforwardly. It is fundamental that the inertness basic conventions keep up steady stage contrasts in the recuperated signs for the whole experiment's runtime.

Currently, we initiate the current hypothesis for the design model of the Synchronizer which would suffice the existing model its practical improvements to establish the accurate phase measurement in real time design environments.

II. LITERATURE REVIEW:

Synchronizer is considered and categorized one of the most important circuitry for the current domain specificity modeling units. Each such modelled units would emphasize on the recurrence in most of current improving technological aspects that would suffice the design criteria. To impart such technological advancements we have acknowledged such changes and which has been improvised in our design criteria. To emphasize on the conditionality criteria of any synchronizer we need to provide some conditionality and its features which would realize the synchronizer would work on stability criteria rather on meta-stability.To emphasize such situations we need to consider specific criteria and its implementation on the large scale design are

ISSN 2347–3657
Volume 7, Issue 4, 2019

tend to prone for multiple errors. We tend to correct such phenomenal problems with particular behavioral criteria which would estimate mathematical modelling of the existing design model utilized in developing the synchronizer. In current era of the digital design techniques, our design manly tend to work on the concepts related to metastability, MST (metastability resolution time) and failure rates. To consider such modelling of the design based on the above operations in synchronizers many researcher have proposed specific design techniques relating the meta-stability and failure rates.

[4] Jerome Cox, George Engel, David Zar, Ian W. Jonesimprovises on cautious synchronizer configuration is basic as System-on-Chip (SoC) items become predominant in security basic applications. Beforehand, utilization of a flip-flop streamlined for information applications was sufficient for most synchronizer utilizes when spread out as a two-organize plan. Expanded requests for both unwavering quality and low-control have uncovered this two-arrange answer for abuse. The acknowledgment that a synchronizer ought to be advanced uniquely in contrast to an information flip-flop opens the structure space to new methodologies. A few precedents are exhibited and two assistants to the procedure are presented.

[5] Vinay S. Thote; Vivek E. Khetade, The important aspect in understanding the multi-clock space framework is the synchronizer. This synchronizer experiences the impact of metastabilityin real time designed circuits and their results in the dis-approval of the circuits utilized. Aversion of the synchronizer from destined valueswhich tend to metastability is attainable. Metastable state happens at whatever point there is an infringement of setup and hold time where the uncontrolled and eccentric variations in information inside setup and hold time window. In this paper, we proposed another engineering of the synchronizer. It distinguishes any advances in information signal inside metastability window. The shut circle increases of the cc (cross-coupled)-invertermodel are constrained by the outside sign. This sign will guarantee the right condition of the synchronizer. The extra piece of the hook comes enthusiastically when this vagueness happens. The accuracy of the circuit usefulness is confirmed utilizing HSPICE and Tanner EDA at the 32nm innovation.

[6] Chang Luo, Jiye Li, Xiaomin Chenproposes a new versatile full computerized bit synchronizer, which utilizes the structure of advanced stage bolted circle contained lead-slack stage finder and direct computerized synthesizer (DDS) is planned dependent on FPGA. The synchronizer has versatile

ISSN 2347–3657
Volume 7, Issue 4, 2019

trademark, so the altered amounts of stage can act naturally modification dependent on distinction of the stage. It has likewise programmable trademark, so recurrence goals, follow step size and stage precision can be set already for the need. The examination results demonstrate that the bit synchronizer has high stage exactness, wide obtaining reach, short hook down time and great adjustment and timing-jitter execution. It very well may be actualized effectively dependent on FPGA.

III. EXISTING MODELED DESIGN UNITS FOR SYNCHRONIZER:

Digital Circuits with metastable criteria's would provide fatal effects for simplest form of design models utilized in circuits such as synchronizers which have to be protected. Considering the reality the synchronizers would require an offbeat input as an input to given plan frameworks where synchronization would not show up will results disappointment in perusing such qualities in every circuit associated with particular structure models. Presently, to ad lib the clock space limits criteria where with various clock areas on a similar designed chips where synchronizers are required when system on chip information crosses the clock area limits. Any flip-failure can undoubtedly be made metastable. Flip its information input at the same time with the inspecting edge of the clock, and you get metastability. One basic approach to show metastability is to sup-handle two timekeepers that vary in all respects marginally in recurrence to the information and clock inputs. Amid each cycle, the general time of the two sign changes a bit, and in the end they change adequately near one another, prompting metastability. This occurrence happens over and over, empowering showing of metastability with ordinary instruments. Getting metastability and the right structure of synchronizers to avoid it is once in a while a craftsmanship. Accounts of glitch and awful synchronizers have to be categorized in certain groups.Synchronizers cannot always be synthesized, they are hard to verify, and often what has been good in the past, have to be developed in futuristic aspects in the design models proposed as below.

3.1 Conventional two flip-flop synchronizer:

More importantly, a traditional two flip-flop synchronizer is utilized for synchronizing a particular singular values utilized in certain circuits. As appeared in Figure 1, considering the current FF (flip-flop) Anand B1 are working in non-concurrent clock space (asynchronous). There is likelihood that while inspecting the info B1-d by FF (flip-flop) failure B1 in CLK_B clock space, yield B1-q may go into metastable state. In any case, amid the one clock cycle time of CLK_B clock, yield B1-q may settle to some steady esteem. Yield of FF(flip-flop) B2 can go

ISSN 2347–3657
Volume 7, Issue 4, 2019

to metastable if B1 does not settle to stable an incentive amid one clock cycle, however likelihood for B2 to be metastable for a total goal clock cycle is near zero. A more

noteworthy number of failure stages might be utilized if recurrence is excessively high as it will help in decreasing the likelihood of synchronizer yield to stay in metastable state.

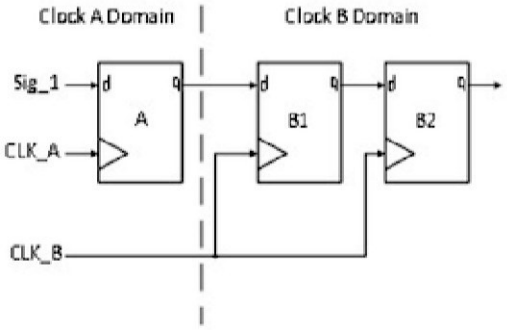


Figure 1: Representing Two FF synchronizer

3.2 Toggle synchronizer

Toggle-Switch synchronizer is utilized to synchronize a heartbeat producing in source clock space to goal clock area. A defined pulse can't be synchronized legitimately utilizing 2 FF synchronizer. While synchronizing from quick clock space to moderate clock area utilizing 2 FF synchronizer, the pulses which can be skipped which can cause the loss of pulses that can be discovered and henceforth ensuing circuit which relies on it, may not work appropriately. Graph in Figure 2 demonstrates switch synchronizer usage.

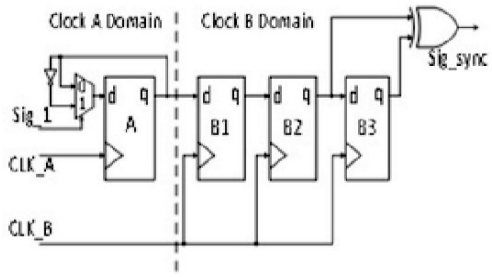


Figure 2: Representing Toggle Synchronizer

3.3 Gray encoding for multi bits signal

At the point when multi bit signals are synchronized with 2-FF(flip-flop) synchronizer, each bit utilized is synchronized utilizing separate 2-FF synchronizer. Metastability can make a flip failure settle down either to a genuine esteem or a bogus esteem. So yield of(designed output of) each synchronizer may not settle to address an incentive at same clock. This causes information incoherency. So as to synchronize multi bit signal utilizing 2 flip-flop synchronizer strategy, just a signgle bit is to defined and the change must be ensured at a specific clock cycle. This can be accomplished by modeled gray encoding. In this way, for instance, in non concurrent FIFO plan, when we synchronize read pointer esteem in the wake of changing over to gray an incentive in compose clock area utilizing 2-FF synchronizer, there is plausibility of metastability. As there is just a single bit change in the grey encoding so regardless of whether there is metastability when

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 7, Issue 4, 2019

clock crossing, the dark counter esteem will be past esteem. For instance, read pointer (dark counter) esteem is changing from 0110 to 0111 and synchronized with compose clock then because of metastability (on the off chance that it happens) plausibility is perused pointer still stays 0110. Presently, assume prior FIFO Full Flag was high at perused dark counter esteem 0110, at that point FIFO Full will stay high for 1 more clock cycle, however this won't cause an issue, in light of the fact that in next clock cycle the read pointer esteem will end up 0111 and FIFO full banner will get de asserted. On the off chance that rather than gray counter digital-valued (binary) counter is taken starting with one clock area then onto the next through two flip failure synchronizer then the multi bit change could cause unpredicted recuperation of various bits after metastability (for example esteem change from "1001" to "1010"). The recuperated read or compose pointer esteem could be incorrect causing incorrectly Flag (FIFO full or FIFO unfilled) age. Figure 3 show how Binary to dark transformation can resolve the issue.

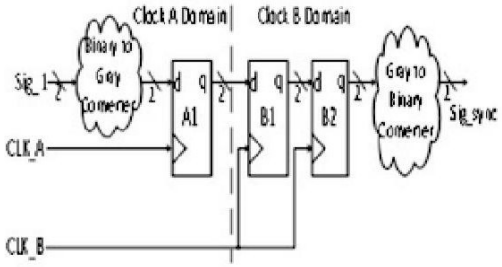


Figure 4: Representing Gray FF Synchronizer

Asynchronous FIFO synchronization

FIFO is most ideal approach to synchronize consistently changing vector information between two non-concurrent clock spaces. Non-concurrent FIFO synchronizer offers answer for exchanging vector signal crosswise over clock area without gambling metastability and coherency issues. In Asynchronous FIFO structure, FIFO gives full synchronization free of clock recurrence. As appeared in Figure 4, read and compose (write) pointers are synchronized to compose and peruse clock areas individually subsequent to performing double to dim change.

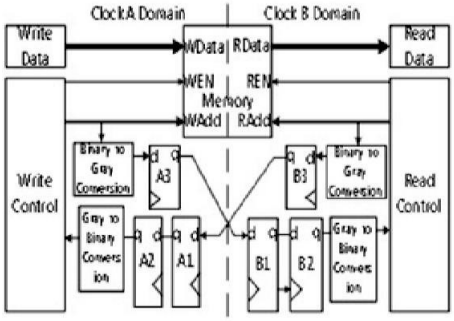


Figure 4: Representing Async FIFO

ISSN 2347–3657
Volume 7, Issue 4, 2019

IV. PROPOSED SYNCHRONIZER DESIGN MODEL

4.1 Introduction to Dual D-FF (Flip-flop) Modelling in Synchronizer

Future SoCs are probably going to comprise of numerous synchronizers on a solitary chip as the quantity of IP centers joined increments. For instance, in a 64-center processor framework, at any rate 128 synchronizers are required by thinking about that one center needs at any rate two synchronizers for its information and yield. In future SoCs, the on-chip correspondence including synchronization, directing and buffering is probably going to influence the framework execution more than handling [18]. As a basic piece of on-chip correspondence organize, the exhibition of the synchronizers on chip is pivotal to the presentation of the whole framework. The least difficult synchronizer involves two flip-flops. Metastability may happen at the principal flip-flop. At that point a full clock cycle is utilized for the metastability to settle. MTBF can be expanded by expanding the clock time frame which is the synchronization time. In any case, the goals of metastability in a two flip-flop synchronizer is generally moderate, which makes it unsatisfactory for fast applications where clock frequencies are high. Before, a wide range of synchronizers with improved execution have been proposed. In any case, they have a typical issue, that is the synchronizer execution corrupts quickly with Vdd diminishing or Vth expanding in light of the fact that the synchronization time steady, τ, which decides the synchronizer execution relies upon the little sign conduct of the bi-stable component in the synchronizers. This circumstance is irritated by bringing down the temperature which results in a higher limit voltage.

Subsequently, the synchronizer execution is touchy to Vdd, Vth and temperature varieties. With the more extensive utilization of intensity sparing procedures, for example, DVFS and the advances in procedure innovation, Vdd will progress toward becoming lower and lower where synchronizers may neglect to work. Moreover, expanding on-chip changeability could fundamentally debase the synchronizer execution. In this way, it is important to plan synchronizers which can work at low Vdd and are vigorous to the Vdd, Vth and temperature varieties.

Anyway before talking about the proposed synchronizer circuits, it is advantageous posing the conspicuous inquiry since, as depicted underneath, synchronizer circuits are risky, along these lines, what might be the MTBF if a synchronizer was excluded, This inquiry can be effectively replied by playing out a straightforward estimation on how frequently a

ISSN 2347–3657
Volume 7, Issue 4, 2019

flip-flop, in a given circumstance, would go into metastability. Consider a flip-flop executed in a 0.18µm CMOS innovation, being driven by a 500 MHz clock, with an information rate of 50 MHz, Assuming Tw is 50 pico-sec, the rate at which metastability happens is$T_w * f_c * f_c$= $50*10^{-12} * 500 * 10^{-6} * 500 *10^{-12}= 1.25* 10^6$.

Henceforth the flip-flop goes into metastability each 800 ns – such a high MTBF can't go on without serious consequences, subsequently the prohibition of synchronizer is definitely not a practical alternative. The inclusion of a synchronizer between two squares in a circuit will clearly result in extra deferral or inactivity in the sign way. Thusly, a portion of the proposed methods were aimed at lessening this postponement or idleness.

One of the regular oversights is to utilize just a solitary flip-flop, which rises to, basically, no synchronizer at all as there will be lacking time for the synchronization procedure to happen bringing about a short MTBF. Another procedure is to synchronize the information bits rather than the control flag with the goal that the handshake convention is stayed away from and therefore the correspondence dormancy is decreased. This plan fizzles on the grounds that every synchronizer may finish up doing various things. Some may accurately test the bit, some may lost the bit and hold the bygone one, and some may enter metastability and resolve to 1 or 0. At last the information examined by consequent circuits is off base. Another drawback of this plan is that it really expands the disappointment rate since the quantity of the synchronizers utilized increments.

4.2 Mathematical Calculations for Design of Dual-D-FIFO Synchronizer:

Firstly, we propose specific parametric criteria's to initiate the design model for the phase measurement design system. Now to improvise such criteria we consider, metastability, MTBF and timing failures.

Criteria forMetastability occurrence:

- When the info signal is an offbeat sign.
- When the clock skew/slew is excessively (rise and fall time are more than the average qualities).
- When interfacing two areas working at two unique frequencies or at a similar recurrence yet with various stage.
- When the combinational postponement is with the end goal that flip-flop information input changes in the basic window (setup+hold window)

[7] MTBF is Mean time between disappointments, Well MTBF gives us data on how regularly a specific component will fall flat or at the end of the day, it gives the normal time interim between two progressive disappointments. The figure

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 7, Issue 4, 2019

beneath demonstrates a commonplace MTBF of a flip-flop and furthermore it gives the MTBF condition. The rundown of various MTBF conditions proposed from 1987 to 2012.

Year	MTBF Unified Model	Comments
1987	$MTBF=\frac{e^{\frac{NT-(N-1)t_{pd}}{\tau}}}{T_W f_c f_d}$	MTBF for N+1 FF synchronizer. Master and slave latches are assumed identical
1992	$MTBF=\tau^N \frac{e^{\frac{NT-2Nt_S^S}{\tau}}}{T_W^{2N} f_c^N f_d}$	MTBF for a N FF synchronizer. Master and slave latches are assumed identical
1997	$MTBF=\frac{e^{\frac{2T-t_{pd}-t_{su}}{\tau}}}{T_W^2 f_c^2 f_d}$	MTBF for a 2 FF synchronizer. Master and slave latches are assumed identical
2003	$MTBF=\frac{e^{\frac{N(T-t_{pd})}{\tau}}}{T_W f_c f_d}$	MTBF for N+1 latches synchronizer. Master and slave latches are assumed identical
2007	$MTBF=\frac{e^{\frac{NT}{\tau}}}{T_W f_c f_d}$	No explicit formula shown
2009		Original formula in paper was for N=4 latches. Result can be extended for N latches
2010	$MTBF=\frac{e^{\frac{N(T-t_{pd})}{\tau}}}{T_W f_c f_d}$	Master and slave latches are assumed identical
2011	$MTBF=\frac{e^{\frac{NT}{\tau}}}{T_W f_c f_d}$	MTBF for a N+1 FF synchronizer. Master and slave latches are assumed identical
2012	$MTBF=(\prod_{i=1}^{N-1}\frac{T_i e^{NT\sum_{i=1}^{N}\frac{1}{\tau_i}}}{T_W^i})\frac{e^{NT\sum_{i=1}^{N}\frac{1}{\tau_i}}}{T_W^N f_c f_d}$	MTBF for a N latches synchronizer

[7] Table1: Representing different postulated formulas for each application designed.

The postulated formula for MTBF is given by:

$$MTBF = \frac{e^{\frac{NT}{r}}}{T_w f_c f_d}$$

Hence we estimate such parametric criteria's to analyze for the each gates connected via its RTL diagram of the design model and resulting its timing analysis.

Hence, to analyze such behavioral changes for each such gates and its circuitry related problems we now consider its design model based on the Toggle and Gray coded synchronizer.

4.3 DESIGN WORKING MODEL:

Our aim on designing specific synchronizer is to establish a correct relation between the entire changes in the phases of the top level design. To establish such real time phase changes we need to consider the synchronizer would not be metastability and has least MTBF. So, in accordance to these parameter we provide the design model as stated below:

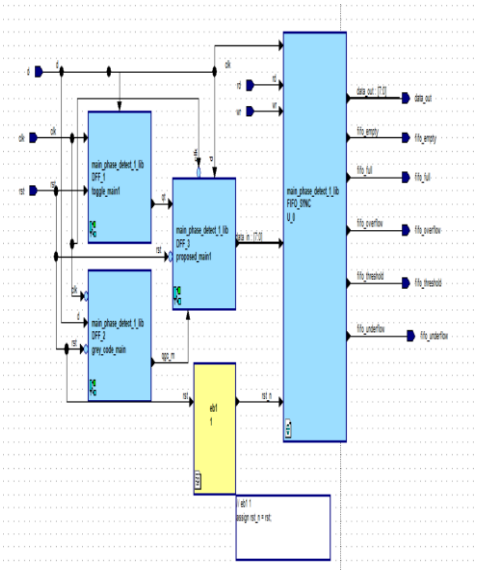


Figure 5: Representing the Proposed block diagram for dual D-FF FIFO Synchronizer.

Now, we utilize three different techniques to initiate the proposed model such as Toggle,

ISSN 2347–3657
Volume 7, Issue 4, 2019

Gray and FIFO Synchronizer which would affect the relation of Metastability. Since, we know that Metastability is directly proportional to the mean time failures which can be estimated correctly depending upon the Flip flop used. Now as we know the our design specializes on Dual-D FF which has better and higher PAD parametric criteria's when considered to normal FF.

Working Scenario of the Hybrid Dual-D FF FIFO synchronizer:

This modeling of the design is observed from the each synchronizer response of the mean time failure and its PAD parameters. Since the existing design models (mentioned III) would suffice the real time aspects parametric criteria which would impart correct scenario for the model and its enhancements based on its.

Hence, we utilize this section of design model to implement the enhanced version of the synchronizer utilized.

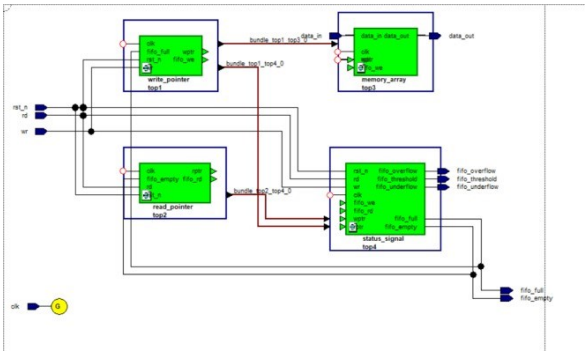


Figure 6: Representing FIFO module Synchronizer with Dual D FF.

The initiation of the design consists of 4 modules such as:

1. Toggle Sync
2. Gray Dual D FF sync
3. FIFO Sync
4. Hybrid Sync

Our aim to provide the data and its implementation on the design modules which would results in correct output which is observed on the same synchronized cycle.

The proposed module is combinatory module for toggle, gray, and FIFO, which would analyzessynchronization process. In our design model, each block module has its purpose to be fulfilled to initiate the synchronized data. For Toggle FF Sync, which aim to provide correct toggled values of the input D changes from 1 to 0 indulging in some or more metastable states, depending upon the no of bits utilized. Since only one bit is utilized and for FF sync to establish corresponding toggle output.

Now, for Gray FF sync, it utilized Register based design technique which are 4 bits data results one or more metastability states. Now we use our design Dual-D FF with FIFO sync to establish correct states observed on the combinatory sync module.

The data for the Dual-D FF FIFO sync would be generated by the combinatory module to

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 7, Issue 4, 2019

establish the correct synchronized data generated from the toggle and gray FF sync.

Hence, utilizing the operations and their limitations of the Exiting synchronizers we could achieve the design much more efficient and elegant model in real time analysis.

4.4 FLOW CHARTS FOR PROPOSED FIFO SYNCHRONIZER BLOCKS:

STATUS SIGNAL BLOCK:

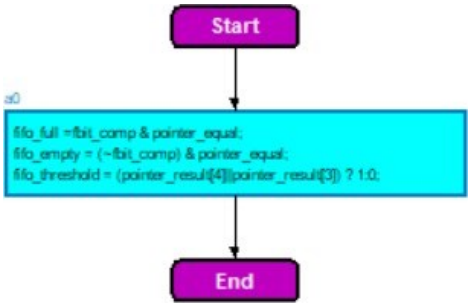


Figure 7: Representing the Status Signal Flow diagram

MEMORY ARRAY:

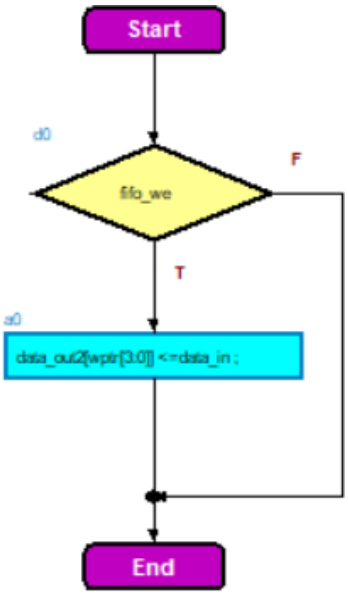


Figure 8: Representing the Memory Array Data Flow diagram

READ POINTER:

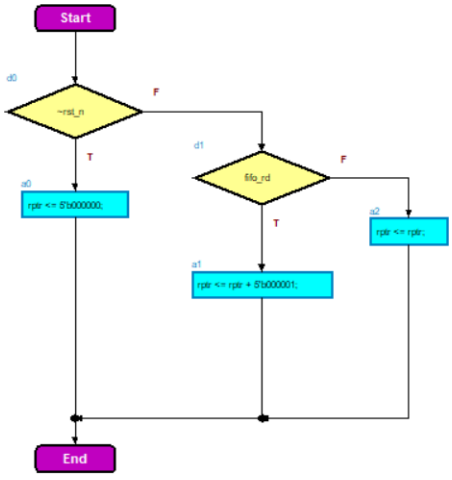


Figure 9: Representing the Read Pointer Flow chart

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 7, Issue 4, 2019

WRITE POINTER:

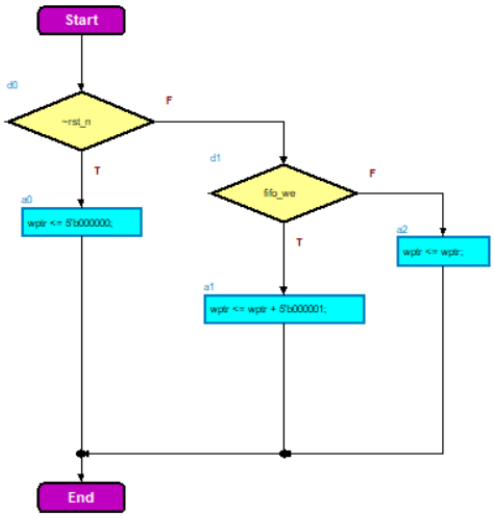


Figure 10: Representing Write pointer Flow diagram

DESCRIPTION:

1. For each changes in the pointer equal and FIFO full condition which would affect the values for the status that have to be updated.
2. Write and Read pointer would rather suffice the values as an incremental and its corresponding values would provide addresses to the temporary memory utilized for storing the synchronized data.
3. Finally the Stored data is displays based on the condition of FIFO empty and full.

RESULTS AND DISCUSSION: In the simulation of the design model we have obtained the results for each modules utilized and their corresponding synthesis results.

SIMULATION RESULTS:

TOGGLE SYNCHRONIZER OUTPUT:

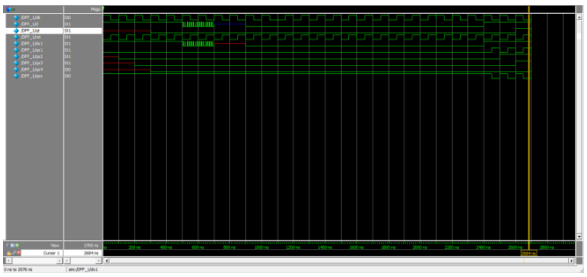


Figure 11: Representing Change in Values of D with respect to the change in values of Respective Flip flops in Toggle Sync.

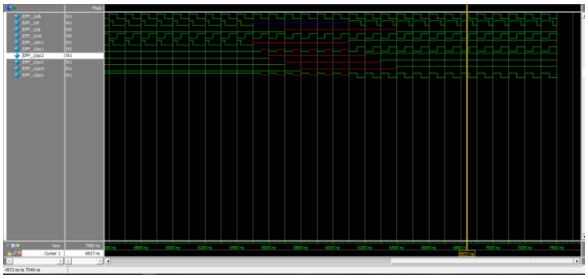
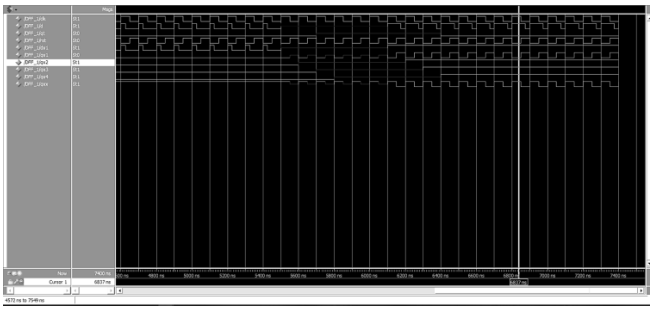


Figure 12: Rst and Clock (clk) conditional values would results in High impedance state

GRAY SYNCHRONIZER OUTPUT:



International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 7, Issue 4, 2019

Figure 13 : Representing the Gray code to binary values changing for the 4 bit Register design

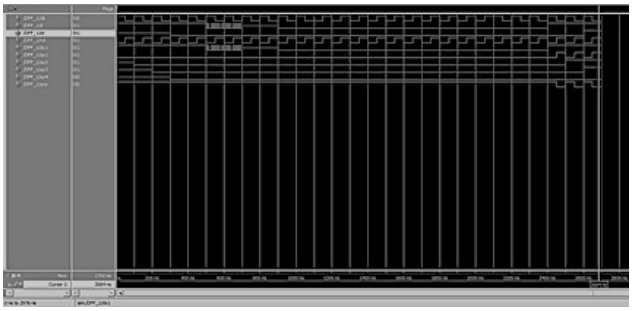


Figure 14: Representing the Data Values generated to the FIFO sync {which is to be modelled using Dual D FF}.

HYBRID DUAL-D FF FIFO Synchronizer:

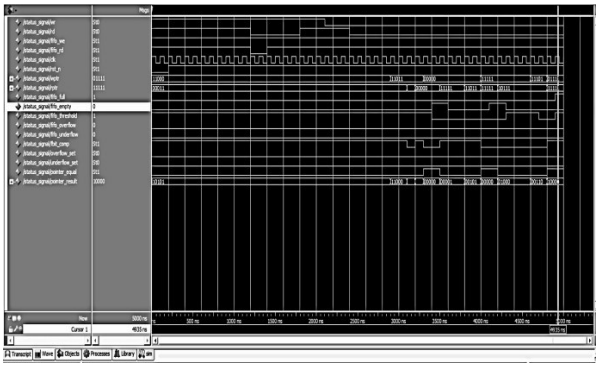


Figure 15: Shows data generated on different values of the FIFO , toggle and Gray FF sync operated on Combinatory module.

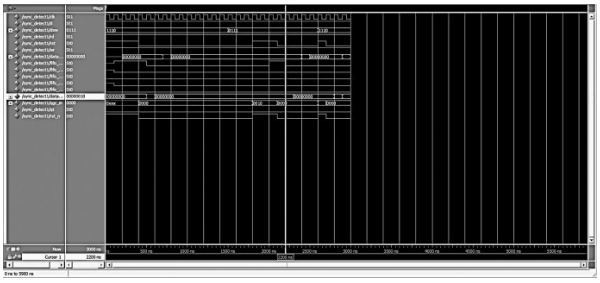


Figure 16: Representing the input observed from the data_in signal for the FIFO sync designed

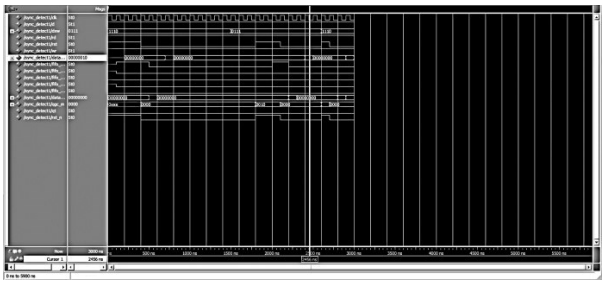


Figure 17: Representing the output signal value in next concurrent phase of the clk signal positive edge triggered.

DESCRIPTION:

1. Figure 11 and 12 would emphasize on the results obtained from the toggle sync where each output its estimated based on the operation of Dual D FF and reverse clock scheme where even and odd modules are given with normal clocking and negative-edge clocking separately.
2. On gray FF sync based on the values of Dwx the values are changed to binary to gray and G-B converter accordingly on the series FF consisting of multiple clocking scheme.
3. Finally for FIFO sync and Combinatory module which consists of D FF modelled flip-flops which utilizes the storage of the data generated form the other two modules accordingly. Hence

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 7, Issue 4, 2019

the correct output is observed in corresponding cycle of the rst values which introduces to change from toggle to FIFO mode.

SYNTHESIS RESULTS:

AREA:

a)

Resource	Utilization	Available	Utilization %
IO	1	500	0.20

b)

Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
LUT	22	133800	0.02
LUTRAM	8	46200	0.02
FF	15	267600	0.01
IO	25	500	5.00
BUFG	1	32	3.12

c)

Resource	Estimation	Available	Utilization %
LUT	30	134600	0.02
LUTRAM	8	46200	0.02
FF	42	269200	0.02
IO	22	500	4.40
BUFG	1	32	3.12

Tables 2 a) Toggle Area Utilization b) FIFO sync utilization area c) Hybrid Dual D FF FIFO sync utilization.

POWER

Toggle Sync:

User Input Data	Confidence	Details	Act
Design implementation state	High	Design is routed	
Clock nodes activity	High	User specified more than 95% of clocks	
I/O nodes activity	High	User specified more than 95% of inputs	
Internal nodes activity	High	User specified more than 25% of internal nodes	
Device models	High	Device models are Production	
Overall confidence level	High		

+-------+-----------+

| Name | Power (W) |

+-------+-----------+

| DFF_1 | <0.001 |

Power Utilized for FIFO Sync:

Power Utilized for Hybrid D-FF FIFO sync.

FORMULATIONS:

Total On-Chip Power:	**0.117 W**
Junction Temperature:	**22.2 °C**
Thermal Margin:	62.8 °C (43.1 W)
Effective ϑJA:	1.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

- DELAY: Route Delay + Logic Delay
- MTBF: $\frac{Number\ of\ FF*clk\_freq}{Failures\ observed\ in\ to\ total}$

TABULATED RESULTS:

SN0	PARAMETERS	EXISITING DESIGN Toggle	FIFO	PROPOSED Dual-D FF FIFO Sync(toggle, FIFO and Gray FF sync)
1	Power(milli Watts)	127	499	117
2	Area (%utilization)	0.2	8.17	7.58
3	Delay(ns)	600	22 ns	63ns
4	MTBF	0.2 ns	80.754 ns	70.805 ns

Table 3: Tabulation of the different parametric conditions for the Existing Synchronizer and Hybrid D-FF FIFO sync.

CONCLUSIONS:

The design of the current hybrid model would improvise a better and novel approach for modelling the sync based on the different limitation observed. Design criteria and its parametric calculation with formulae have been

ISSN 2347–3657
Volume 7, Issue 4, 2019

mentioned and the resulting values observed from the Xilinx software would suffice the estimation. Each considered parameters have been observed and tabulated accordingly.

FUTURE SCOPE:

Implementing the Hybrid FIFO synchronizer its real time scenario on Xilinx FPGA board Virtex series.

The back end model and its implementation on Microwind and its implementation of the design in real time applications such as phase detection and FPGA circuits.

REFERENCES

[1]R. Ginosar,"Metastability and synchronizers: A tutorial,"IEEE Design & Test of Computers, vol. 28, no. 5, pp.23-35, 2011.

[2] N. Agrawal; Y. Kimura,R. Arghavani; S. Datta, "Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III–V Semiconductor) on Variation for Logic and SRAM Applications," Electron Devices, IEEE Transactions on , vol.60, no.10, pp.3298,3304, Oct. 2013.

[3] W.J. Dally, S.G. Tell, "The Even/Odd Synchronizer: A Fast, All-Digital, Periodic Synchronizer," ASYNC, pp. 75-84, 2010.

[4] Jerome Cox, George Engel, David Zar, Ian W. Jones"**Synchronizers and Data Flip-Flops are Different**"[5]**Vinay S. Thote ; Vivek E. Khetade** "**Modified synchronizer for protection from metastability**" 20-21 May 2016 IEEE International Conference on Recent

Trends in Electronics, Information & Communication Technology (RTEICT) **Electronic ISBN:** 978-1-5090-0774-5

[6] Chang Luo ;Jiye Li ; Xiaomin Chen "**A new adaptive bit synchronizer based on DDS**" 16-18 April 2011 International Conference on Consumer Electronics, Communications and Networks (CECNet)**Print ISBN:** 978-1-61284-458-9

[7]Ang Boon Chong eASIC Corp"**Product Level MTBF Calculation**"2014 Fifth International Conference on Intelligent Systems, Modelling and Simulation2166-0662/14 $31.00 © 2014 IEEEDOI 10.1109/ISMS.2014.137