International Journal of Information Technology & Computer Engineering

ISSN 2347–3657

Volume 14, Issue 1, 2026

Designing High Speed 8bit vedic multiplier using Brent Kung Parallel Prefix Adder

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Abstract: *The need for high-speed arithmetic operations in modern digital systems, particularly in processors and signal processing units, has led to the exploration of efficient multiplier architectures. This paper presents the design and implementation of a high-speed 8-bit Vedic multiplier integrated with a Brent-Kung parallel prefix adder for optimized performance. Vedic multiplication, derived from ancient Indian mathematics, offers significant advantages in terms of speed and regularity due to its recursive Urdhva Tiryagbhyam (vertical and crosswise) algorithm. To further enhance computation speed, the final addition stage of partial products employs the BrentKung adder — a logarithmic time complexity adder known for its minimal logic depth and reduced fan-out compared to other parallel prefix adders. The proposed architecture is modeled using Verilog HDL and synthesized using Xilinx Vivado. Comparative analysis demonstrates that the combination of Vedic multiplication and Brent-Kung addition achieves lower delay, reduced area, and improved power efficiency when compared to traditional array multipliers and ripple carry adder-based implementations. The results validate that the design is wellsuited for high-speed applications in embedded systems, digital signal processors, and cryptographic hardware. A high-speed 8-bit multiplier architecture based on Vedic mathematics is presented, utilizing the Urdhva Tiryagbhyam sutra for efficient partial product generation. To further accelerate the computation process, the final addition of partial products is performed using the Brent-Kung parallel prefix adder, known for its logarithmic delay and minimal fan-out, making it suitable for high-speed arithmetic circuits. The integration of Vedic multiplication with the Brent-Kung adder significantly reduces propagation delay, area, and power consumption when compared to conventional multiplier architectures employing ripple carry adders or carry-save adders. The proposed design is described in Verilog HDL and synthesized using Xilinx Vivado for performance evaluation. Simulation results demonstrate improved speed and resource utilization, highlighting the proposed architecture's suitability for realtime and embedded signal processing applications.*

Keywords: *VHDL, Xilinx, Vedic.*

Introduction

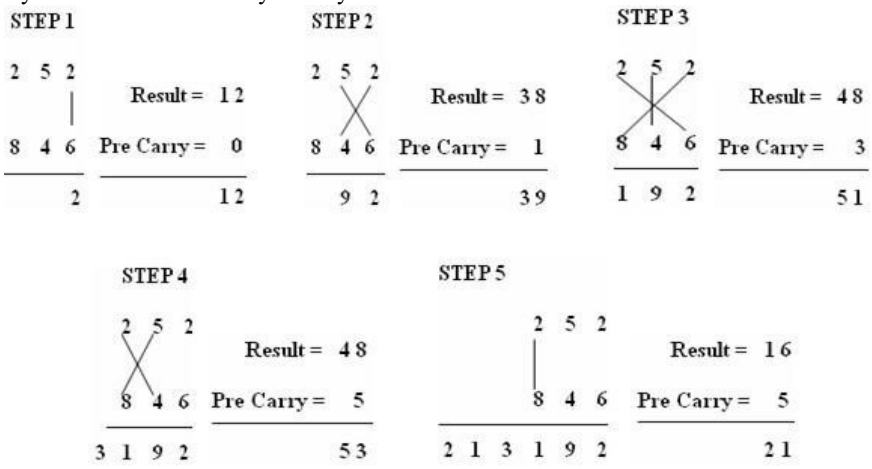
Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1]. The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors. This paper describes the design and implementation of 4x4 bit Vedic multiplier UrdhvaTiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics using EDA (Electronic Design Automation) tool. The paper is organized as follows. Section 2 describes the basic methodology of Vedic multiplication technique. Section 3 describes the hardware architecture of 2x2 and 4x4 bits Vedic Multiplier (VM) based on Vedic multiplication.

The use of Vedic mathematics lies in the fact that it reduces the typical form of calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing

The proposed Vedic multiplier is based on the "Urdhva Tiryakbhyam"sutra(algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 14, Issue 1, 2026

products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers. To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 * 846 by Urdhva Tiryakbhyam method as shown in figure.



252 x 846 = 213192

FIG 1 Multiplication of two decimal numbers

Literature Survey

Efficient multiplier design remains a cornerstone of high-performance compute systems, including digital signal processors, microprocessors, and image processing units. Traditional multiplication techniques such as shift-and-add, array multipliers, and Booth's algorithm are commonly used but suffer from higher propagation delays and greater hardware complexity when scaled to higher bit-widths. Recent advancements have turned towards Vedic mathematics, particularly

The Urdhva Tiryakbhyam Sutra, a technique that enables parallel generation of partial products and is well-suited for digital hardware implementation. As demonstrated in various studies [1], [2], Vedic multipliers offer significant speed advantages and reduced area over conventional approaches. Their hierarchical and modular structure makes them especially favorable for FPGA implementation and hardware reuse.

To further accelerate computation, integration of high-speed adders has become essential in optimizing the final addition of partial products. The Brent-Kung adder, a type of parallel prefix adder, is known for its low fan-out, logarithmic delay, and minimal gate count compared to other adders such as Kogge-Stone or CarryLookahead adders [3]. This makes it highly suitable for performance-sensitive applications, striking a balance between speed, area, and power consumption. Hybrid architectures combining Vedic multipliers with parallel prefix adders have been explored to capitalize on both algorithmic efficiency and fast carry propagation. Studies have indicated that these hybrid systems outperform traditional multiplier structures, particularly in 4-bit and 8-bit designs [4], [5]. However, limited research has focused specifically on the integration of 8-bit Vedic multipliers with Brent-Kung adders, a niche addressed by the current work.

Moreover, recent developments in FPGA technology have encouraged real- testing and validation of such architectures. Researchers have successfully implemented Vedic multipliers on platforms such as Xilinx Spartan-3 and Spartan-6, reporting reduced critical path delay and LUT utilization [6]. The modularity of the Vedic approach, when combined with the predictable structure of Brent-Kung adders, results in a highly scalable and efficient arithmetic design.

Existing System

The hardware architecture of 2x2 and 4x4 bit Vedic multiplier (VM) modules are displayed in the below sections. Here, “Urdhva-Tiryakbhyam” (Vertically and Crosswise) sutra is used to propose such an architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay.

Vedic Multiplier for 2x2 bit

The method is explained below for two, 2 bit numbers *A* and *B* where A = a1a0 and B = b1b0 as shown in Figure 2. Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 14, Issue 1, 2026

higher multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

Multiplier is a major block in designing digital systems. Several algorithms are reported in literature to implement fast multipliers. VEDIC multiplication algorithm is another option to implement an efficient multiplier. This work discuses the VEDIC multiplier. There are 3 methods to implement multiplication in VEDIC mathematics. Out of three, only one method is generic method which can be applied to all cases whereas other two are for special cases. Main algorithm of Vedic multiplication is Urdhva Triyakbhyam.

Problem Statement

The project "Design of High-Speed 8-bit Vedic Multiplier Using Brent-Kung Adders" aims to address the growing need for efficient and high-speed arithmetic operations in digital systems. Multiplication is a fundamental operation in various applications such as digital signal processing (DSP), cryptography, image processing, and machine learning algorithms, where speed and accuracy are crucial. Conventional multipliers, such as array multipliers and shift-and-add multipliers, are often slow and consume considerable power, especially for larger bit-widths.To overcome these limitations, the project proposes the design of an 8-bit Vedic multiplier, leveraging Vedic mathematics, known for its faster and more efficient multiplication techniques.

The Vedic method significantly reduces the time complexity compared to traditional multiplication algorithms. In this project, the Vedic multiplier will be enhanced using Brent-Kung adders, a type of parallel-prefix adder that is known for its minimal delay and efficient carry propagation. By combining the fast computation abilities of the Vedic multiplication technique with the low-latency Brent-Kung adder, the goal is to design a high-speed 8-bit multiplier that improves performance in terms of both speed and are.

The below figure shows the vedic multiplier using ripple carry adder

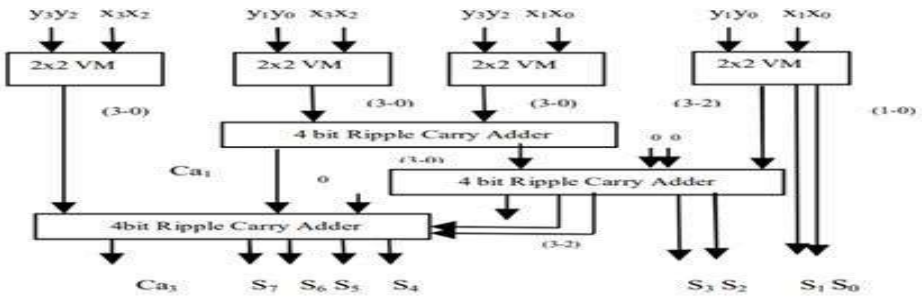
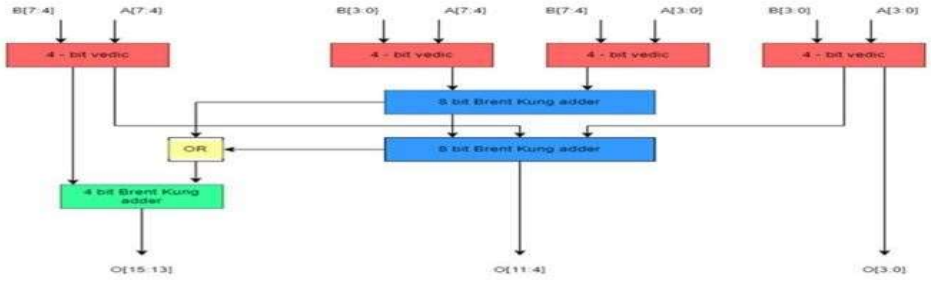


FIG 2 Existing System Using Ripple Carry Adder

Proposed System

The disadvantage with the existing model is that it uses ripple carry adder to compute the sum. Thus using these will increase the propagation delay. The adder with less delay and area is implemented using Brent Kung adder . The second problem with the existing architecture is that it uses three n-bit adders to compute the result. Thus, in modified architecture we use two n-bit adders and one (n/2)-bit adder. The hardware required for proposed Vedic Multiplier using Brent Kung adder will be reduced and delay also be reduced The prefixes for 2 bit groups are calculated by the Brent Kung adder. With the assistance of these prefixes, it is possible to determine the prefixes for 4 bit sets, which are then used to determine the prefixes for 8 bit groups, and so on. In order to calculate the carry out of a specific bit stage, these prefixes are next needed. The Sum bit for that phase will be calculated using these carries and the Group Propagate of the following stage.



International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
Volume 14, Issue 1, 2026

FIG 3 Proposed System Using Brent Kung Parallel Prefix Adder

Results And Discussion

In this chapter, we will discuss about the results of the Designing High Speed 8bit vedic multiplier using Brent Kung Parallel Prefix adder

Working

The 8-bit input sequence is divided into two 4-bit numbers and given as inputs to the 4bit multiplier blocks (a[7:4] & b[7:4], a[3:0] & b[7:4], a[7:4] & b[3:0], a[3:0] & b[3:0]). The four multipliers used are similar and give 8-bit intermediate products which are added using overlapping logic with the help of three Brent–Kung (BK) adders. The partial products obtained from the four multipliers are demarcated into four regions. The four LSB product bits P[3:0] are directly obtained from one of the multipliers. The output of the second and third multiplier block is added directly using BK adder -1 as the second and third region is overlapping. Then the higher order bit of first multiplier block is added to the overlapping sum using BK adder-2 which gives the product P[7:4]. Finally, MSB bits P[15:8] are obtained by adding the fourth multiplier output to the carry from BK adder -1 (added at the fifth bit position) and higher order bits (acts as lower nibble of addend) of BK adder -3.

Results

The area is shown in the form of LUT(look up tables) and IO resources

Resource	Utilization	Available	Utilization %
LUT	101	41000	0.25
IO	32	300	10.67

FIG 4: Utilisation Table Of Vedic Multiplier

The area consumed is also less compared with previous work hence we can say that The multipllier using brent kung parallel prefix adder is more efficient.

Simulation Results

The product of 8bit is being shown below. The two inputs are being given than the product of them is shown .

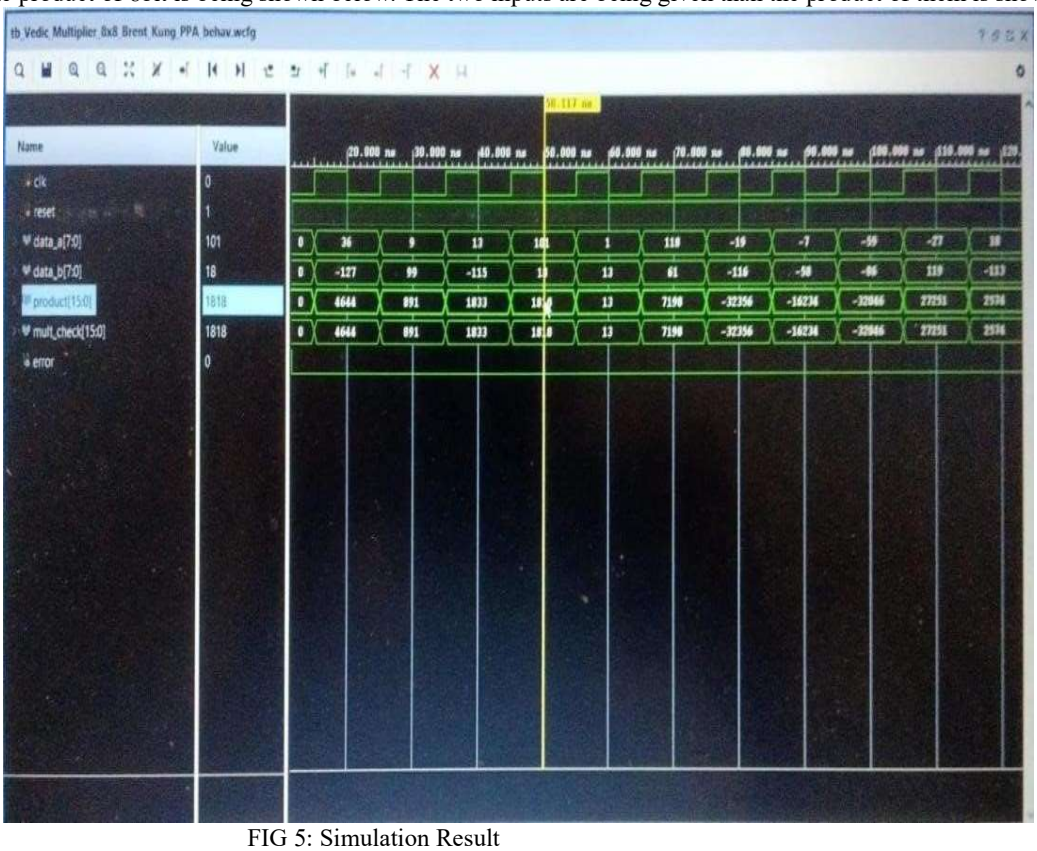


FIG 5: Simulation Result

International Journal of Information Technology & Computer Engineering
ISSN 2347–3657
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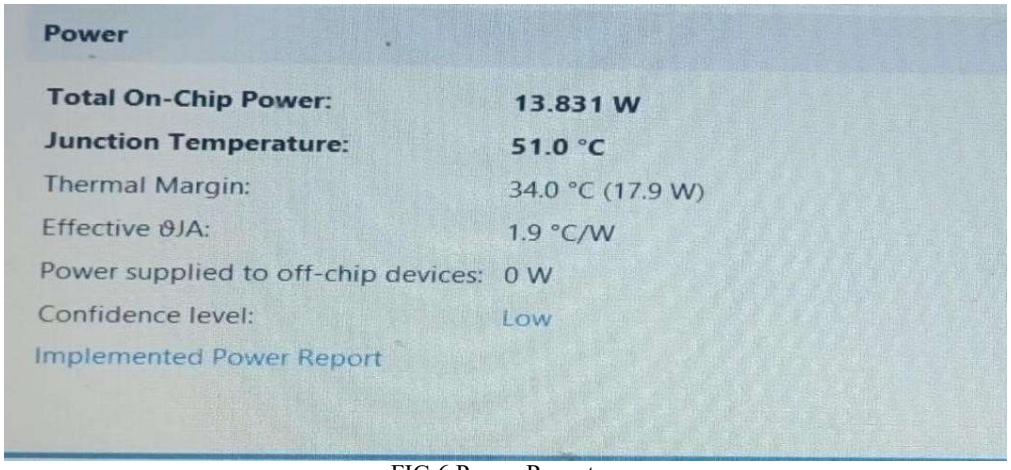


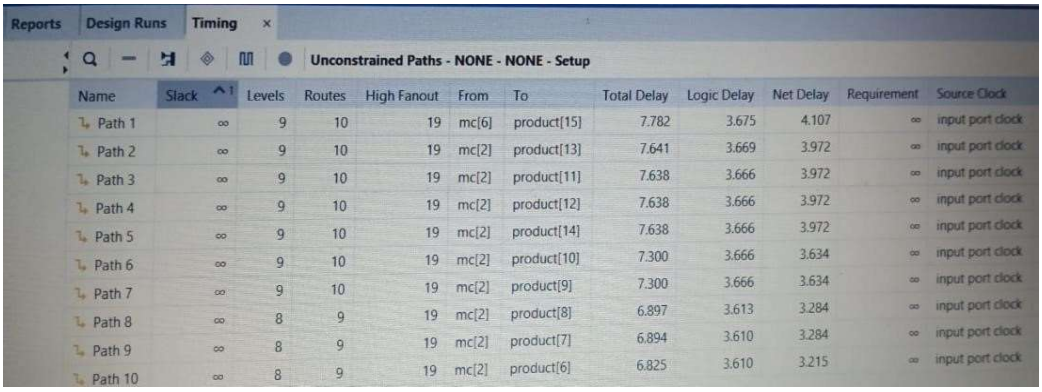
FIG 6 Power Report

The power reading of the above are 13.321 which is less compared to previous Works hence we The below are the comparisons with the previous work can that the power consumed less. And the system is more efficient And one of the advantage . And also the area consumed also less.

REFERENCES	DESIGN TYPE	SIZE	AREA(LUT)	POWER(W)	DELAY
R.Sharma and Agarwal (2017)	Array multiplier	8bit	192	15,98	32.01
R.Bend and h kung (2019)	Booth multiplier	8bit	123	18.64	29.543
A.Kumar and sharma (2020)	Kogge and adder	8bit	117	37.15	70.2
Proposed work	Brent Kung adder	8bit	101	13.831	3.610

FIG 7 Previous Work Report

Critical Delay



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	9	10	19	mc[6]	product[15]	7.782	3.675	4.107	∞	input port clock
Path 2	∞	9	10	19	mc[2]	product[13]	7.641	3.669	3.972	∞	input port clock
Path 3	∞	9	10	19	mc[2]	product[11]	7.638	3.666	3.972	∞	input port clock
Path 4	∞	9	10	19	mc[2]	product[12]	7.638	3.666	3.972	∞	input port clock
Path 5	∞	9	10	19	mc[2]	product[14]	7.638	3.666	3.972	∞	input port clock
Path 6	∞	9	10	19	mc[2]	product[10]	7.300	3.666	3.634	∞	input port clock
Path 7	∞	9	10	19	mc[2]	product[9]	7.300	3.666	3.634	∞	input port clock
Path 8	∞	8	9	19	mc[2]	product[8]	6.897	3.613	3.284	∞	input port clock
Path 9	∞	8	9	19	mc[2]	product[7]	6.894	3.610	3.284	∞	input port clock
Path 10	∞	8	9	19	mc[2]	product[6]	6.825	3.610	3.215	∞	input port clock

FIG 8 Critical Delay

Conclusion

In conclusion, this chapter explored the operation, and results of the project.

In 8-bit Vedic multiplier, designed using the Urdhva Tiryagbhyam sutra and Brent-Kung parallel prefix adder, offers a good balance of speed and area efficiency. By leveraging the inherent parallelism of the Vedic multiplication algorithm and the efficient carry propagation of the Brent-Kung adder, this design achieves faster computation compared to traditional methods, while also keeping the hardware complexity manageable. The simulation results often demonstrate reduced delay, power consumption, and area compared to other multiplier architectures.

Future scope

The future scope of designing 8bit vedic multiplier using brent kung parallel prefix adder is enhancing performance, exploring hardware implementations, and extending the design to more complex applications and emerging technologies. Further optimization can be achieved by integrating adaptive architectures, approximate computing techniques, and exploring quantum and neuromorphic computing domains.

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