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Memory Built-in Self Test(MBIST) for ROM

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Abstract
The reliability of embedded memory has become a major concern in modern System-on-Chip (SoC) designs, where a significant portion of the silicon area is occupied by memory blocks. Read-Only Memory (ROM), which stores firmware and configuration data, must be thoroughly verified to avoid functional failures after fabrication and during field operation. Conventional memory testing techniques based on external test equipment are costly and unsuitable for at-speed and in-system verification.
This paper presents the design and implementation of a Memory Built-In Self-Test (MBIST) architecture dedicated to ROM. The proposed approach employs a compact on-chip controller, address sequencing logic and a signature analysis unit to verify the correctness of ROM contents without external support. A modified read-only March-based access strategy is adopted, and the read responses are compressed using a Multiple Input Signature Register (MISR). The generated signature is compared with a pre-computed golden signature to determine the pass or fail status of the memory.
The complete architecture is described in VHDL and verified using Xilinx ISE tools. Simulation results confirm correct functionality of the controller, signature generation and pass/fail decision logic. The proposed MBIST scheme offers low hardware overhead, supports at-speed testing and enables periodic in-field diagnostics, making it suitable for reliability-critical embedded systems.

Keywords: *MBIST, ROM testing, MISR, signature analysis, March algorithm, VHDL, embedded memory.*

1. Introduction

Embedded memories play a dominant role in contemporary digital systems and SoC platforms. Among them, Read-Only Memory (ROM) is widely used to store boot code, firmware and configuration tables that are essential for correct system operation. Any defect in ROM, such as incorrect cell programming, address decoder errors or signal integrity faults, can lead to permanent system malfunction.

As semiconductor technology scales and integration density increases, the likelihood of manufacturing-induced defects in memory structures also increases. Traditional memory testing relies on Automatic Test Equipment (ATE), which applies test patterns externally after fabrication. Although this method is effective for basic validation, it suffers from high cost, long test time and limited capability to perform at-speed and in-system testing.

Built-In Self-Test (BIST) techniques provide an attractive alternative by embedding test circuitry directly within the chip. In particular, Memory Built-In Self-Test (MBIST) architectures enable autonomous verification of embedded memory blocks and are now considered an essential part of modern design-for-test strategies.

While MBIST techniques are well established for RAM, ROM testing introduces unique challenges because its contents cannot be modified after fabrication. Therefore, ROM-oriented MBIST must rely exclusively on read and comparison operations using known data relationships. This paper focuses on the development of a lightweight MBIST architecture specifically designed for ROM verification using signature analysis.

2. Related Work

Early research on built-in self-test introduced linear feedback shift registers and signature analysis for reducing test data and simplifying output response evaluation. Subsequent work extended these concepts to memory testing by incorporating address generators, finite-state controllers and dedicated response analyzers.

The March family of memory test algorithms has been widely adopted due to its structured access order and high fault coverage. Several variants such as March C- and March SS are known to detect common fault models, including stuck-at, transition and coupling faults. However, for ROM, conventional write operations are not applicable. Researchers have therefore proposed read-only adaptations in which memory responses are verified

against expected patterns or compressed into signatures.

Recent studies emphasize the importance of compact MBIST controllers and signature analyzers to reduce area overhead while preserving sufficient diagnostic capability. The use of MISR-based response compression has been shown to be effective in detecting pattern-sensitive and address-related faults in read-only memories.

The present work builds on these established principles and implements a ROM-specific MBIST architecture using a deterministic address sequence and MISR-based signature comparison.

3. Proposed MBIST Architecture for ROM

3.1 Overall Structure

The proposed MBIST architecture consists of the following major components:

- MBIST controller
- Address counter
- ROM under test
- Multiple Input Signature Register (MISR)
- Signature comparison and status logic

The controller coordinates the entire test sequence, enabling address generation and data capture while monitoring test completion.

3.2 MBIST Controller and Address Generation

The controller is implemented as a finite-state machine. When a test request or reset event occurs, the controller initiates the test procedure and enables the address counter. The counter sequentially scans the complete ROM address space, ensuring that every memory location is accessed exactly once during a test cycle.

This deterministic access order simplifies the generation of the expected signature and ensures repeatability of the test.

3.3 Response Compression Using MISR

The ROM output data are fed into a Multiple Input Signature Register. The MISR is realized using an XOR-based feedback structure similar to a linear feedback shift register. For every ROM access, the output data are compacted into the register state.

At the end of the test sequence, the MISR holds a final signature that represents the cumulative response of the ROM for the applied access pattern. This technique avoids the need to store or directly compare large volumes of read data.

3.4 Signature Comparison and Status Logic

A predefined golden signature, generated from a fault-free ROM model, is stored in the comparison logic. After completion of the address sweep, the generated MISR signature is compared with the golden reference. If both values match, the ROM is declared fault-free; otherwise, a failure flag is asserted.

The final test result is stored in a status register and can be accessed by on-chip software, diagnostic hardware or external test interfaces.

3.5 Test Methodology

The adopted test strategy follows a read-only adaptation of March-style access ordering. The methodology includes:

1. Sequential traversal of all ROM addresses.
2. Read operation at each address.
3. Incremental response compaction using the MISR.
4. Final signature comparison against the reference value.

This approach enables detection of common ROM fault classes such as stuck-at faults, decoder faults and coupling-related anomalies.

4. Implementation Flow

The complete MBIST architecture was described in VHDL and integrated with the ROM model. The design flow includes:

- RTL modeling of the controller, counter, MISR and status logic
- Functional simulation of fault-free operation
- Verification of controller sequencing and signature generation
- Pass/fail flag validation

Xilinx ISE 14.7 was used for synthesis and simulation. The modular structure allows the MBIST logic to be easily reused or adapted for different ROM sizes.

5. Results and Discussion

RTL synthesis confirms correct structural integration of the MBIST controller, ROM interface and signature analyzer. Functional simulations demonstrate that the address counter correctly traverses the entire memory space and that the MISR accumulates ROM responses synchronously with read operations.

The final status signal asserts a successful pass when the generated signature matches the golden reference. When altered data patterns are introduced in the ROM model, the resulting signature differs and the failure flag is correctly asserted. These results confirm the effectiveness of the proposed architecture in identifying memory inconsistencies.

The hardware overhead is limited to a small controller, counter and MISR block, making the approach suitable for embedded systems where area and power budgets are constrained.

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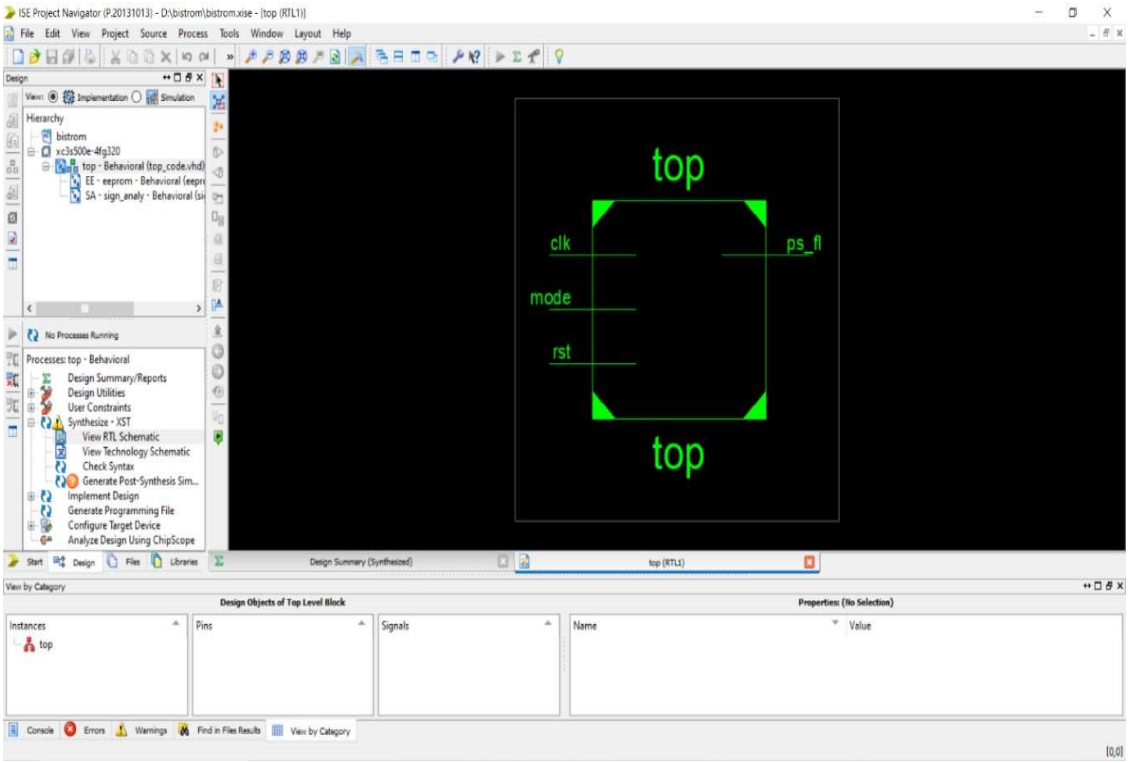

Fig 1:RTL schematic view

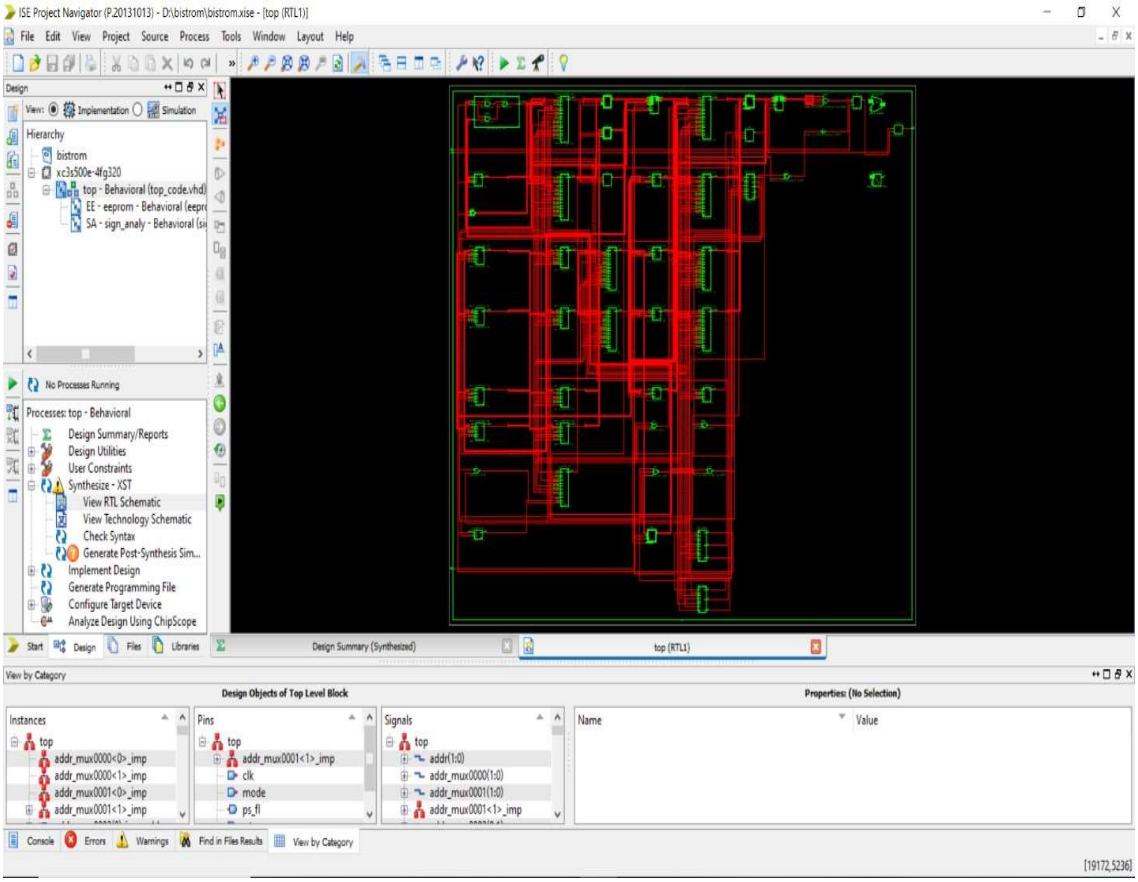

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Fig 2: Internal view of RTL block

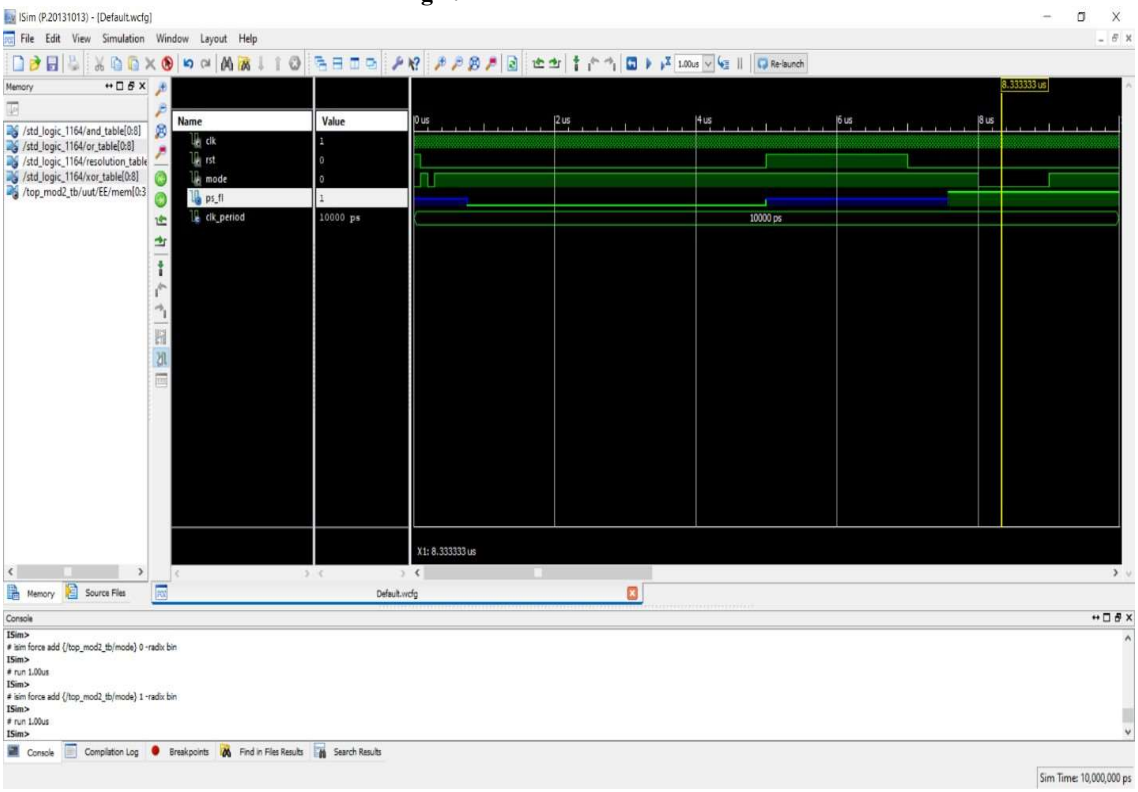

Fig 3: Simulation result

6. Advantages and Limitations

6.1 Advantages

- Eliminates dependency on external test equipment
- Supports at-speed and in-system testing
- Low hardware and power overhead
- Enables periodic self-diagnostics during field operation
- High detection capability for common ROM fault models

6.2 Limitations

- ROM testing is restricted to read-only operations
- Fault localization is limited due to response compression
- Additional design and verification effort is required to integrate MBIST logic

7. Applications

The proposed MBIST architecture is applicable to a wide range of systems, including:

- microprocessors and microcontrollers for firmware verification,
- automotive electronic control units,
- medical and safety-critical embedded platforms,
- secure systems requiring ROM-based boot and key validation, and
- low-power IoT devices requiring autonomous diagnostics.

8. Conclusion and Future Work

This paper presented a compact and efficient MBIST architecture for Read-Only Memory. By combining deterministic address sequencing with MISR-based signature analysis, the proposed design enables autonomous and at-speed verification of ROM contents without external test infrastructure. Simulation results confirm the correct operation of the controller, response analyzer and pass/fail logic. Future work will focus on extending the architecture to support multiple memory instances and heterogeneous memory types such as SRAM and Flash. Further improvements may include enhanced diagnostic resolution, low-power test scheduling and integration with SoC-level safety and reliability monitoring frameworks.

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