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Performance Analysis of 2D FET with Diverse Dielectrics For Low Power

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ABSTRACT

In recent years, two-dimensional field effect transistors (2D FETs) have attracted considerable attention as promising candidates for next-generation electronic devices. This work presents a detailed performance analysis of 2D FETs employing channel materials such as MoS_2, $MoSe_2$, $MoTe_2$, and WS_2, evaluated with different dielectric layers for low-power electronic applications. These materials belong to the transition metal dichalcogenide (TMD) family and exhibit unique electronic characteristics, including suitable band gaps, high carrier mobility, and strong electrostatic control, making them ideal for nanoscale transistor channels.The study examines the effect of various dielectric materials, including conventional silicon dioxide (SiO_2) and high-k dielectrics such as hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and air. Key device performance parameters analyzed in this work include subthreshold swing, ON/OFF current ratio, transconductance, drain voltage versus carrier density, carrier velocity versus drain voltage, and gate capacitance versus gate voltage. The results indicate that the selection of dielectric material significantly influences device behavior, where high-k dielectrics—particularly HfO_2—demonstrate improved electrostatic control and reduced power consumption compared to SiO_2.Additionally, the intrinsic properties of MoS_2, $MoSe_2$, $MoTe_2$, and WS_2, including their direct and indirect bandgap characteristics, play an important role in determining overall transistor performance. The interface quality between the 2D channel and dielectric layer is also evaluated, as it directly affects carrier transport and switching efficiency. Simulation outcomes reveal that combining TMD-based channels with high-k dielectric materials enhances subthreshold characteristics and overall energy efficiency. These findings highlight the strong potential of 2D FETs for future low-power integrated circuit applications.

Keywords: *2D Field Effect Transistors (2D FETs), Transition Metal Dichalcogenides (TMDs), MoS_2, $MoSe_2$, $MoTe_2$, WS_2, High-k Dielectrics, Hafnium Oxide (HfO_2), Aluminum Oxide (Al_2O_3), Silicon Dioxide (SiO_2), Nanoelectronics, Low-Power Devices, Subthreshold Swing, ON/OFF Current Ratio, Transconductance, Carrier Mobility, Gate Capacitance, Energy Efficient Electronics.*

INTRODUCTION

The progress of modern electronics is closely linked to the continuous development of transistor technology. Since their invention, transistors have undergone remarkable transformation aimed at achieving reduced dimensions, enhanced performance, and minimized power consumption. As conventional silicon-based devices approach their physical and scaling limitations, two-dimensional field-effect transistors (2D FETs) have emerged as promising alternatives for next-generation semiconductor technologies.

The origin of transistor technology dates back to the mid-twentieth century with the invention of the bipolar junction transistor (BJT). Subsequently, the introduction of the metal–oxide–semiconductor field-effect transistor (MOSFET) revolutionized integrated circuit design. Due to their scalability, low power operation, and reliability, MOSFETs became the backbone of modern electronic systems. However, aggressive scaling of silicon MOSFETs has introduced challenges such as short-channel effects, increased leakage current, and power dissipation issues, limiting further miniaturization.

To overcome these limitations, researchers have explored atomically thin materials for transistor channels. Two-dimensional materials such as graphene and transition metal dichalcogenides (TMDs), including molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), molybdenum ditelluride ($MoTe_2$), and tungsten disulfide (WS_2), have attracted considerable attention. These materials exhibit desirable properties such as tunable bandgaps, high carrier mobility, strong electrostatic control, and excellent thermal stability. Such characteristics make them suitable candidates for low-power and high-performance transistor applications.

The development of 2D FETs is primarily driven by the need to enhance device efficiency while reducing energy consumption. Their atomic thickness allows superior gate control over the channel, thereby suppressing leakage currents and improving switching characteristics. These advantages make 2D FETs particularly attractive for low-power electronic applications. Consequently, the transition from bulk silicon transistors to 2D material-based devices represents a significant

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milestone in semiconductor evolution and highlights the ongoing pursuit of technological advancement.

1.2 Scattering Transport

Carrier transport in semiconductor devices can generally occur in two modes: scattering transport and ballistic transport. These transport mechanisms describe how charge carriers move within the channel region and interact with imperfections in the material. The nature of transport significantly influences the electrical performance of electronic devices.

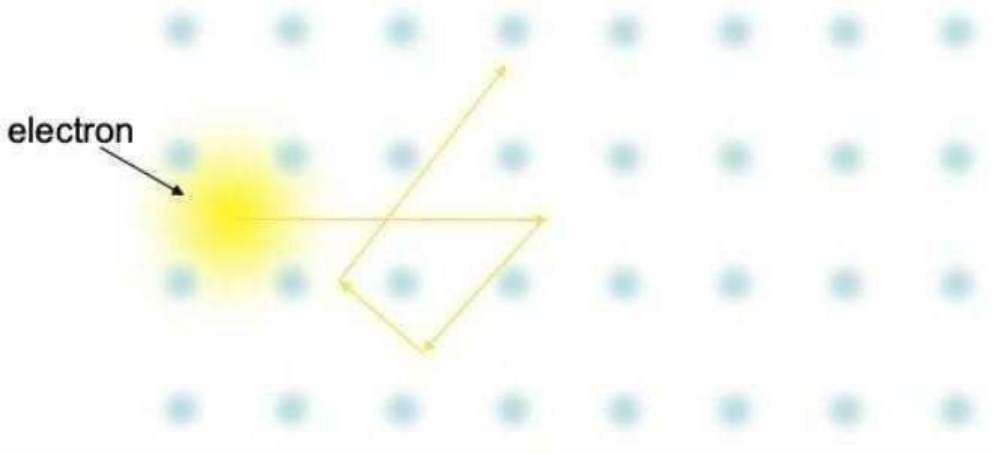

Fig ; Scattering Transport

In practical 2D FET structures, scattering transport is commonly observed, especially in low-power configurations. In this mode, charge carriers experience collisions with phonons, impurities, surface irregularities, and other imperfections. These scattering events reduce carrier mobility and influence current flow. Minimizing such scattering mechanisms is essential for improving device efficiency and reducing energy dissipation.

Ballistic transport, in contrast, occurs when carriers move through the channel with minimal or no scattering. This mode is typically associated with ultra-short channel devices and high-speed applications. However, achieving pure ballistic transport is difficult in practical devices due to unavoidable imperfections and thermal vibrations.

Several scattering mechanisms influence electron transport in semiconductor materials:

Lattice Scattering: Interaction between electrons and lattice vibrations (phonons) reduces carrier mobility, particularly at higher temperatures.

Impurity Scattering: Dopant atoms introduce localized energy states that disturb carrier movement and affect conductivity.

Surface Scattering: Interface roughness between the semiconductor and dielectric layers leads to scattering and mobility degradation.

Grain Boundary Scattering: In polycrystalline materials, grain boundaries interrupt carrier flow and alter electrical characteristics.

Electron–Electron Scattering: Coulomb interactions between carriers become significant at high carrier concentrations.

Magnetic Scattering: Magnetic impurities or external magnetic fields influence electron trajectories.

Defect Scattering: Structural defects such as dislocations and vacancies interfere with carrier transport.

Boundary Scattering: In nanoscale devices, electrons interact with edges and boundaries, leading to quantum transport effects.

Understanding these mechanisms is essential for optimizing 2D FET performance and achieving efficient low-power operation.

Scaling Revolution

Continuous scaling has been the driving force behind advancements in semiconductor technology. As transistor dimensions shrink, higher device density and improved performance can be achieved. However, conventional silicon devices face physical and electrostatic limitations at nanometer dimensions. Two-dimensional materials offer a promising solution to extend scaling beyond traditional limits.

The atomic thickness of 2D materials provides excellent electrostatic control and reduced short-channel effects. This enables faster switching, lower leakage currents, and improved energy efficiency. Materials such as MoS_2, $MoSe_2$, $MoTe_2$, and WS_2

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play an important role in achieving ultra-scaled transistor designs. Additionally, their favorable thermal properties support efficient heat dissipation in compact devices.

Despite these advantages, challenges remain in fabrication, material integration, and contact resistance. Quantum effects also become more prominent as device dimensions decrease. Researchers are actively investigating novel architectures and fabrication techniques to address these challenges. The scaling revolution of 2D FETs is therefore expected to play a vital role in shaping future low-power and high-performance electronic systems.

Problem Statement

The continuous scaling of field-effect transistors introduces several technical challenges that affect performance, reliability, and manufacturability. Issues such as increased leakage current, reduced gate control, short-channel effects, and heat dissipation limit the efficiency of conventional devices. These challenges necessitate the exploration of alternative materials and device structures.

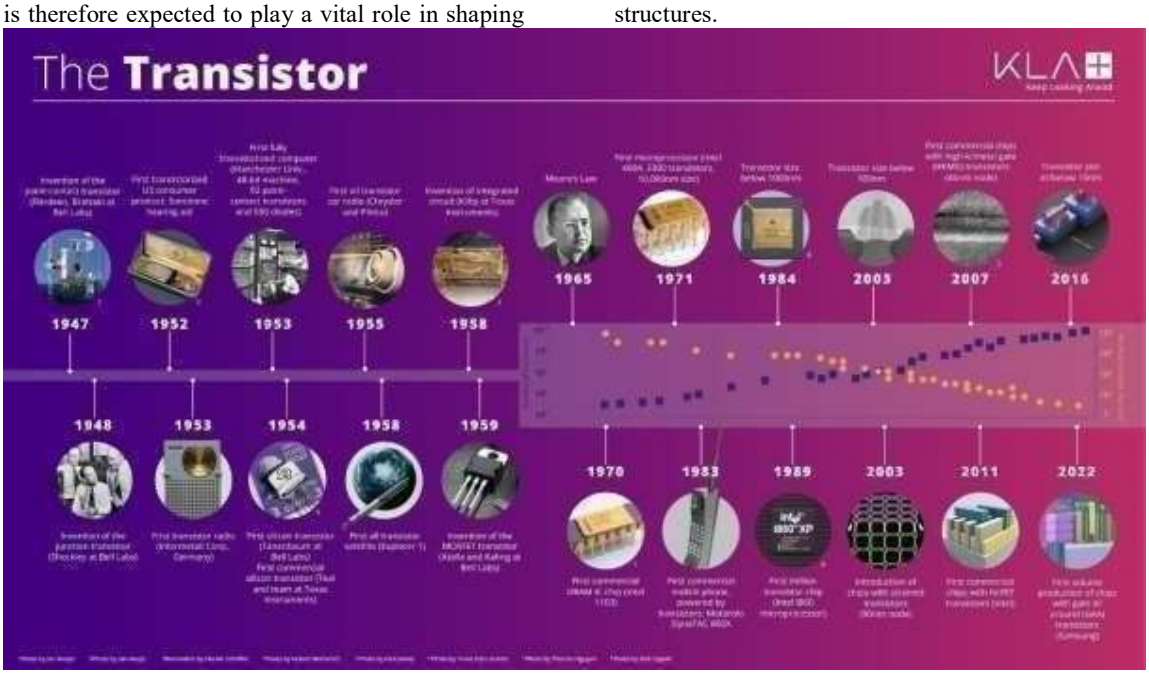

Fig : Evolution of Transistors

This work focuses on improving the performance of 2D FETs by analyzing the influence of different parameters, including:

1. Channel length
2. Channel materials (MoS_2, $MoSe_2$, $MoTe_2$, WS_2)
3. Dielectric materials

By optimizing these parameters, the study aims to enhance device efficiency and enable low-power operation.

Objectives

The primary objective of this work is to analyze the performance of 2D field-effect transistors using different dielectric materials for low-power applications. The study aims to evaluate how dielectric selection influences key device characteristics and overall energy efficiency.

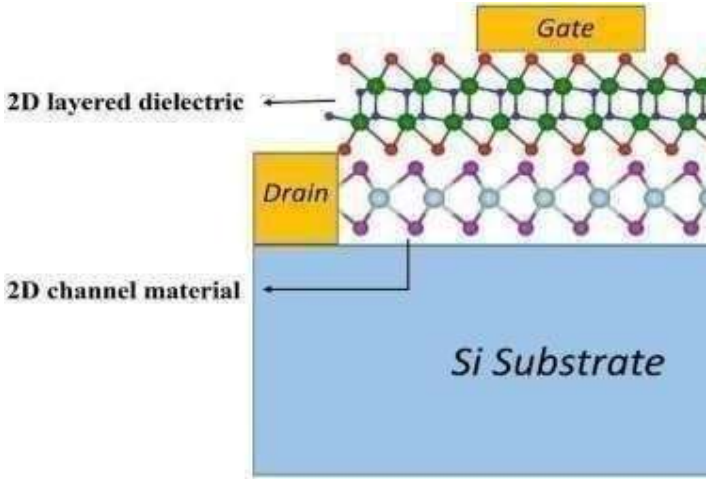

Fig : 2D FET Structure

The specific objectives include:

- Investigating the impact of various dielectric materials on 2D FET performance
- Evaluating power consumption and switching characteristics

- Analyzing subthreshold swing and ON/OFF current ratio
- Studying device scalability at reduced channel dimensions
- Comparing performance of different TMD channel materials
- Optimizing gate stack configurations for improved efficiency
- Identifying suitable dielectric-channel combinations for low-power operation

This analysis provides insights for designing energy-efficient electronic devices using 2D materials.

EXISTING MODEL

Transition Metal Dichalcogenides (TMDs)

Transition metal dichalcogenides (TMDs) have emerged as promising materials for next-generation electronic devices, particularly in low-power transistor applications. These materials, including molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), molybdenum ditelluride ($MoTe_2$), and tungsten disulfide (WS_2), possess a layered two-dimensional structure composed of a transition metal layer sandwiched between two chalcogen layers. Their atomically thin nature allows improved electrostatic control and reduces short-channel effects, which is essential for low-power device operation.

One of the most important characteristics of TMDs is their tunable bandgap. For instance, MoS_2 exhibits an indirect bandgap in bulk form but transitions to a direct bandgap semiconductor when thinned to a monolayer. This property makes TMDs highly suitable for transistor applications where efficient switching and reduced power consumption are required. Additionally, several TMD materials demonstrate relatively high carrier mobility compared to traditional semiconductor materials at nanoscale dimensions, enabling faster carrier transport and improved device performance.

The semiconducting nature of TMDs also contributes to low off-state current (Ioff), which is critical for minimizing standby power consumption. When used as channel materials in field-effect transistors, the atomic thickness of TMD layers enhances gate control over the channel region. This leads to improved switching behavior and reduced leakage current. Furthermore, TMDs are compatible with high-k dielectric materials, which further enhances electrostatic control and supports efficient low-power operation.

Another advantage of TMD materials is their scalability. Their ultra-thin structure enables continued device miniaturization while maintaining acceptable electrical characteristics. This scalability aligns well with the ongoing demand for compact and energy-efficient integrated circuits. Therefore, TMD-based devices offer significant potential for future low-power electronics, sensors, and high-density integrated circuit applications.

Dielectrics

Dielectric materials play a crucial role in transistor operation by electrically isolating the gate electrode from the channel while allowing capacitive coupling. The choice of dielectric material significantly affects threshold voltage, gate control, leakage current, and overall transistor performance. As device dimensions shrink, selecting appropriate dielectrics becomes increasingly important for maintaining efficient operation.

The dielectric constant, commonly represented by k or ε, indicates the ability of a material to store electrical energy in an electric field. Materials with different dielectric constants influence the capacitance between the gate and channel, thereby affecting device switching characteristics. In this study, dielectric materials with constants such as $k = 1$ (air), $k = 3.9$ (SiO_2), $k \approx 7.5$ (Al_2O_3/nitride), and $k \approx 22$ (HfO_2) are considered.

Air, with a dielectric constant close to unity, provides minimal capacitance. Although not typically used as a gate dielectric in practical devices, it is useful for comparison and for applications requiring low parasitic capacitance. Silicon dioxide (SiO_2), with a dielectric constant of approximately 3.9, has traditionally been used as a gate dielectric due to its good insulating properties and compatibility with semiconductor fabrication processes. It provides a balance between capacitance and insulation, making it suitable for conventional transistor designs.

Dielectrics with moderate dielectric constants, such as aluminum oxide or nitride materials, offer improved capacitance compared to SiO_2 while maintaining acceptable leakage characteristics. These materials are beneficial for enhancing gate control in scaled devices. High-k dielectrics such as hafnium oxide (HfO_2), with dielectric constants around 22, significantly increase gate capacitance without requiring extremely thin physical layers. This helps reduce leakage current and improve electrostatic control, which is particularly advantageous for low-power 2D FETs.

The selection of dielectric materials directly influences device performance parameters such as subthreshold swing, ON/OFF current ratio, and power consumption. High-k dielectrics improve gate coupling, while lower-k materials reduce parasitic capacitance depending on application requirements. Therefore, proper dielectric engineering is essential for optimizing 2D FET performance and achieving energy-efficient transistor operation.

TOOL USED

The platform **NanoHUB.org** is widely recognized as an important resource in the field of nanotechnology. It provides an integrated

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environment that supports researchers, students, and educators by offering simulation tools, learning materials, and collaborative opportunities related to nanoscience and nanoscale engineering. These facilities help users design, analyze, and understand nanoscale systems more effectively.

One of the major strengths of the platform is its collection of simulation and modeling tools. These tools enable users to study the behavior of materials and devices at the nanoscale without requiring expensive laboratory equipment. Through virtual experiments, researchers can analyze material properties, predict system performance, and develop nanoscale components. This capability significantly reduces development time and supports innovation in nanotechnology-based research.

Another important feature of the platform is the availability of educational resources. NanoHUB provides lecture notes, tutorials, online courses, and instructional modules covering various nanotechnology topics. These materials help students build foundational knowledge while also assisting educators in incorporating modern nanotechnology concepts into their curriculum. As a result, the platform supports both learning and teaching activities in a structured manner.

Fig : Tool Logo

In addition to technical and educational support, NanoHUB promotes collaboration among users. The platform includes discussion forums, shared workspaces, and networking options that allow researchers and learners to exchange ideas and work together. This collaborative environment encourages knowledge sharing and often leads to joint research activities, improving the overall quality of projects.

Simulation Interface

The platform also provides access to datasets and research publications related to nanotechnology. Users can review recent studies, analyze available data, and stay updated with ongoing developments in the field. This access to current research information is essential for conducting meaningful and relevant work in nanoscience.

Another significant advantage of NanoHUB is its accessibility. Being a web-based platform, it allows users to access tools and learning materials from any location with an internet connection. This flexibility enables students and researchers to perform simulations, learn concepts, and collaborate with others without geographical limitations. Such accessibility makes NanoHUB a valuable tool for academic and research purposes in nanotechnology.

SIMULATION ANALYSIS AND RESULTS

The simulation of the proposed nanoscale transistor structure was carried out using carefully selected device parameters. These parameters were chosen to evaluate the electrical behavior of different transition metal dichalcogenide (TMD) channel materials under nanoscale conditions. The values used in the simulation are summarized in Table 4.1.

Table: Device Parameters

Simulation Parameter	Value
Channel Materials	MoS_2, $MoSe_2$, $MoTe_2$, WS_2
CMOS Type	n-type (electron channel)
Channel Direction	X-direction
No. of Fins	3 nm
Transport Model	With Scattering
Dielectrics	1 – 22
Gate Length	5 nm – 10 nm
Ambient Temperature	300 K
Gate Voltage Sweep	0 V – 0.7 V (15 Steps)
Drain Voltage Sweep	0 V – 0.7 V (15 Steps)

These parameters were selected to investigate device performance at ultra-scaled gate lengths while considering realistic scattering effects and temperature conditions.

Circuit Diagram

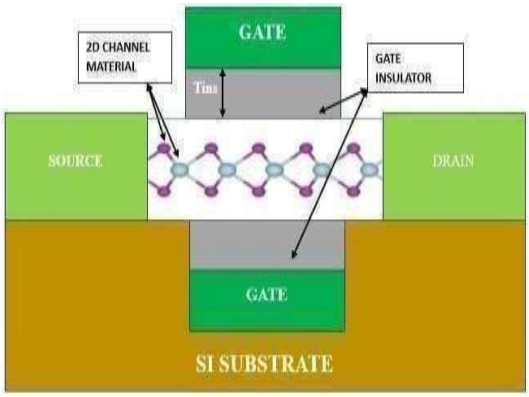

Fig ; Circuit Diagram

The simulated device structure and biasing configuration used for analysis are illustrated in Fig. 4.1. The circuit diagram represents the nanoscale MOSFET structure with gate, source, and drain terminals configured for voltage sweep simulations.

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Quantum Capacitance and Drain Current Characteristics

Quantum Capacitance vs Gate Voltage and Drain Current vs Gate Voltage

The variation of quantum capacitance with respect to gate voltage is shown in Fig. 4.2. The results indicate that quantum capacitance increases gradually as the gate voltage rises. At higher gate voltages, the curve tends to saturate due to the limited density of states in the channel material. In contrast, the ideal reference curve continues to increase linearly, which does not account for quantum confinement effects. This deviation highlights the importance of considering quantum capacitance in nanoscale device modeling.

The drain current versus gate voltage characteristics also demonstrate typical transistor switching behavior. At lower gate voltages, the drain current increases exponentially, representing the subthreshold conduction region. As the gate voltage increases further, the current reaches saturation, indicating strong channel formation. The difference between ideal and simulated curves reflects non-ideal phenomena such as carrier scattering and quantum capacitance effects.

Drain Current vs Drain Voltage Characteristics

Drain Current vs Drain Voltage

Figure 4.3 illustrates the relationship between drain current (Id) and drain voltage (Vd) for multiple gate voltage values. For each gate bias, the drain current initially increases linearly with drain voltage, representing the linear operating region. Beyond a certain drain voltage, the current saturates, which corresponds to channel pinch-off and saturation mode operation.

The results also show that higher gate voltage values produce larger drain currents. This behavior occurs because increased gate voltage strengthens the inversion layer, enhances carrier concentration, and reduces channel resistance. Consequently, the device allows greater current flow under higher gate bias conditions.

Gate Voltage vs Average Carrier Velocity

Gate Voltage vs Average Velocity

The variation of carrier average velocity with gate voltage is presented in Fig. 4.4. At very low gate voltages, carriers exhibit relatively high velocity due to minimal scattering effects. As the gate voltage increases, the average velocity decreases sharply, which indicates enhanced scattering and stronger carrier interaction within the channel.

Beyond approximately 0.05 V, the carrier velocity stabilizes and remains nearly constant. This saturation suggests that further increases in gate voltage do not significantly influence carrier transport speed, primarily due to velocity saturation effects commonly observed in nanoscale devices.

Transconductance Efficiency (gm/Id) Analysis

The gm/Id versus gate voltage curve demonstrates the efficiency of the device for analog and digital applications. At low gate voltages, particularly in the subthreshold region (Vg < 0.3 V), the gm/Id ratio remains high. This indicates superior transconductance efficiency, which is desirable for low-power analog circuit design.

As the gate voltage increases, the gm/Id ratio decreases rapidly and eventually stabilizes at lower values. This behavior corresponds to the strong inversion region where the device operates with higher current but reduced efficiency. Such characteristics are suitable for high-speed digital switching applications.

SIMULATION RESULTS

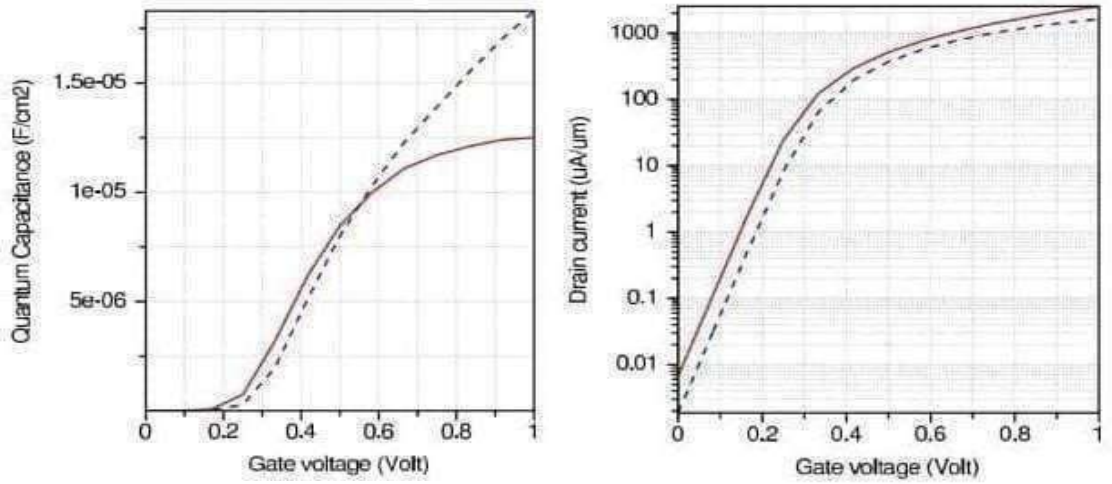

Fig 4.2: Quantum Capacitance vs Gate Voltage and Drain Current vs Gate

Voltage

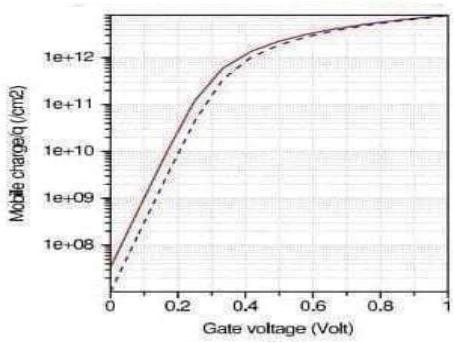

Fig 4.3: Drain Current vs Drain Voltage

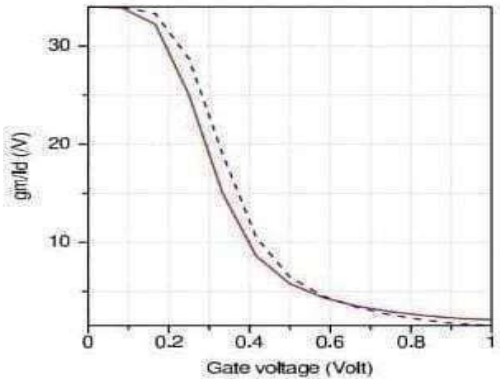

Fig 4.4: Gate Voltage (V) vs Average Velocity

Advantages

The evaluation of dielectric materials in two-dimensional field-effect transistors offers several performance benefits. Proper dielectric selection enables reduced leakage current and optimized dynamic power consumption, which is essential for low-power electronic systems. By studying dielectric behavior, the device can be designed to operate efficiently while maintaining minimal energy loss.

Another key advantage is improved device scalability. As transistor dimensions continue to shrink into the nanometer regime, dielectric materials play a critical role in maintaining device performance. The analysis provides insight into how dielectric properties influence short-channel effects and overall transistor reliability at extremely small gate lengths.

Dielectric materials also affect switching characteristics. By choosing appropriate dielectric layers, better gate control can be achieved, which improves switching speed and enhances transistor performance. Strong electrostatic control further helps in minimizing short-channel effects such as drain-induced barrier lowering (DIBL) and improves subthreshold slope.

High-κ dielectric materials contribute to reduced gate leakage current by increasing gate capacitance without requiring extremely thin oxide layers. This allows improved device efficiency while maintaining reliable insulation between gate and channel. In addition, dielectric evaluation supports compatibility studies between 2D semiconductor materials such as MoS_2 and WS_2 and various dielectric layers, ensuring better interface quality.

Thermal performance is another important benefit. Suitable dielectric selection helps improve heat dissipation in compact nanoscale devices, thereby enhancing operational stability. Furthermore, dielectric properties influence threshold voltage

behavior. Careful analysis allows selection of materials that provide stable threshold voltage across different operating conditions.

Finally, optimized dielectric materials help achieve higher ON/OFF current ratios. This improves switching reliability and reduces standby power consumption, which is essential for modern low-power electronic circuits.

Disadvantages

Despite the advantages, several challenges are associated with dielectric analysis in 2D FETs. One major limitation is the complexity of material integration. Two-dimensional channel materials and advanced dielectric layers often exhibit lattice mismatch, which may introduce interface defects and reduce device reliability during fabrication.

Another drawback is the high computational requirement for simulation. Modeling nanoscale devices involves solving quantum transport equations and electrostatic interactions, which demands significant computational power and simulation time.

Compatibility issues also arise when certain high-κ dielectric materials interact chemically or thermally with 2D semiconductors. Such incompatibilities may degrade interface quality and affect electrical performance. Additionally, achieving consistent experimental results remains challenging due to variations in fabrication processes such as deposition techniques and material synthesis. These variations may lead to differences between simulated and practical device characteristics.

Conclusion

The selection of dielectric materials plays a significant role in determining the performance of two-dimensional field-effect transistors. From the simulation analysis, it is evident that dielectric properties strongly influence gate control, leakage current, switching characteristics, and overall device efficiency. Materials such as MoS_2 and WS_2 demonstrate favorable electrical behavior, good compatibility with 2D channels, and reduced scattering effects, making them suitable for low-power nanoscale transistor applications.

However, the optimal dielectric choice depends on device requirements, including operating voltage, channel material, and performance targets. Other materials such as $MoSe_2$, $MoTe_2$, and WSe_2 may offer advantages in specific applications where different electrical or thermal properties are required. Therefore, dielectric selection must be carefully optimized based on the intended application.

Overall, the study confirms that dielectric engineering is essential for improving the performance and scalability of nanoscale 2D FET devices. Proper material selection leads to enhanced switching behavior, improved electrostatic control, and reduced power consumption.

Future Scope

Future research can focus on exploring new two-dimensional dielectric materials and heterostructures with tailored electrical characteristics. Investigating advanced fabrication methods to minimize interface defects will further improve device reliability. In addition, large-scale integration techniques must be developed to enable commercial deployment of 2D material-based devices.

Further work can also examine alternative device architectures such as tunnel field-effect transistors and multi-gate structures for achieving ultra-low power operation. Studies on long-term reliability, thermal management, and device stability under practical operating conditions will be essential for real-world applications. These research directions will contribute to the development of next-generation low-power electronic systems based on two-dimensional materials.

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