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Design Of Frequency Divider Using MEML

Kazi Nikhat Parvin[1], Gutti Anjali[2], Racharla Ashwitha[3], Ayyannagari Manogna[4]
[1]Associate Professor; Department Of Electronics And Communication Engineering Bhoj Reddy Engineering College For Women, Hyderabad, India.
[2,3,4]B.Tech Students ; Department Of Electronics And Communication Engineering Bhoj Reddy Engineering College For Women, Hyderabad, India.
Mail Id; anjali.g.h95@gmail.com[2],ashwitharacharla@gmail.com[3], ayyannagarimanogna@gmail.com[4]

Abstract
High-frequency communication systems require efficient circuits for frequency synthesis and signal processing. Among these circuits, frequency dividers play an important role in applications such as phase-locked loops, wireless transmitters, and I/Q signal generators. This paper presents the design and implementation of a frequency divider using MOS Current Mode Logic (MCML). MCML is widely recognized for its high-speed switching capability, reduced voltage swing, and improved noise immunity, making it suitable for high-frequency and low-power integrated circuits.In this work, the proposed frequency divider is designed and simulated using the Cadence Virtuoso environment based on 180 nm CMOS technology. The circuit architecture focuses on achieving high operational speed, compact layout area, and efficient power utilization. The divider operates by producing an output signal whose frequency is a predetermined fraction of the input signal frequency.

The differential signaling nature of MCML contributes to enhanced signal integrity and reduced switching noise, which are critical for reliable operation in high-frequency systems. In addition, the design provides strong fundamental frequency suppression while maintaining low power dissipation, making it suitable for portable and wireless electronic applications. Simulation results demonstrate the effectiveness of the proposed design in terms of speed, power consumption, and accuracy of frequency division.

Keywords— *Frequency Divider, MOS Current Mode Logic (MCML), CMOS Technology, High-Speed Circuits, Low Power Design, Phase-Locked Loop (PLL), Cadence Virtuoso, Differential Signaling.*

Introduction

Frequency dividers are essential components in high-frequency integrated circuits and are widely used in phase-locked loops (PLLs), I/Q generators, clock recovery systems, and wireless transmitters. These circuits are commonly implemented either as standalone blocks or cascaded stages within frequency synthesis architectures. As operating frequencies increase into the gigahertz range, conventional CMOS logic encounters limitations due to large voltage swings and switching noise. To address these challenges, MOS Current Mode Logic (MCML), also referred to as Source Coupled Logic (SCL), is frequently adopted for high-speed applications where both speed and area efficiency are critical.

Although MCML provides superior high-frequency performance, it suffers from relatively high static power consumption due to constant bias current operation. In practical PLL implementations, the first divider stage in the feedback loop may consume a significant portion of the total current budget of the frequency synthesizer. Technology scaling improves digital CMOS circuits; however, MCML circuits operating at gigahertz frequencies behave more like analog circuits due to sampling and latching mechanisms. Consequently, the benefits of technology scaling are not immediately realized in MCML-based designs.

To improve performance, optimization techniques for MCML latches and logic gates are required. These techniques aim to maintain adequate noise margin while minimizing power consumption and ensuring stable differential pair operation. Analytical modeling of transistor current–voltage and capacitance characteristics enables improved sizing of transistors. In particular, transistor width can be expressed as a function of drain current using square-law relations associated with transconductance. Proper modeling is important because the optimal MCML design depends strongly on the accuracy of these relationships.In this work, each latch in the divider is optimized based on its actual load conditions to reduce total power consumption. Instead of relying solely on fixed voltage gain requirements, oscillation amplitude and voltage gain are treated as design variables. This approach may slightly degrade the noise margin; however, in RF frequency divider applications, continuous toggling and locking mechanisms reduce the impact of occasional edge loss compared to data processing circuits.

CMOS Technology

Complementary Metal-Oxide-Semiconductor (CMOS) technology is one of the most widely used semiconductor technologies for integrated circuit design. It is extensively utilized in microprocessors, memory devices, application-specific integrated circuits (ASICs), microcontrollers, and communication systems. CMOS employs complementary pairs of PMOS and NMOS transistors, enabling efficient logic operation with low static power consumption.

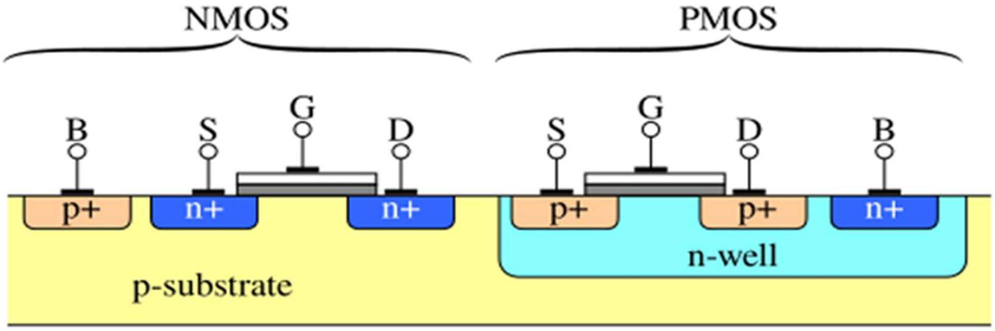


Figure 1 CMOS

Unlike NMOS or bipolar technologies, CMOS circuits dissipate negligible static power because current flows only during switching events. This characteristic enables high integration density and improved performance. CMOS technology is therefore suitable for large-scale digital systems.

MOS Current Mode Logic (MCML)

To reduce switching noise in high-speed circuits, techniques such as reduced voltage swing and current steering are employed. Several alternative logic families have emerged to improve mixed-signal compatibility. These logic families are categorized into single-ended and differential structures.

Single-ended families such as Current Steering Logic (CSL) minimize current transients during switching. Differential families, including Complementary Current Balanced Logic (CCBL), Folded Source Coupled Logic (FSCL), and Current Mode Logic (CML), provide improved noise immunity by balancing signal transitions.

MCML is a differential logic style that maintains constant current flow and reduces switching noise. Unlike CMOS circuits, which generate transient current spikes during switching, MCML circuits exhibit steady current behavior. This characteristic makes MCML suitable for high-speed mixed-signal and RF circuit applications.

Working of MCML

The basic MCML inverter consists of a differential NMOS pair, load resistors, and a constant current source. The differential pair performs the logic operation, while the load resistors determine output voltage swing. The constant current source provides bias current for the circuit.

SOFTWARE REQUIREMENTS

This chapter describes the software tools required for the design and simulation of the frequency divider using MOS Current Mode Logic (MCML). The selection of an appropriate Electronic Design Automation (EDA) tool is essential for designing high-speed digital circuits, performing simulations, and analyzing performance parameters. In this work, Xilinx Vivado is used as the primary design platform because it provides a comprehensive environment for digital design entry, simulation, synthesis, and implementation. The tool allows designers to develop complex digital systems efficiently and evaluate performance before hardware realization.

Software Requirements

Figure 2 Vivado Icon

Xilinx Vivado is an integrated software suite developed for designing and implementing digital circuits on field-programmable gate arrays (FPGAs) and adaptive computing platforms. It offers a complete workflow that supports hardware description, simulation, synthesis, placement, routing, and debugging. Vivado is widely used in academic and industrial environments due to its flexibility, advanced optimization capabilities, and support for high-performance digital system design. The tool enables designers to describe circuits using hardware description languages such as VHDL, Verilog, and SystemVerilog, as well as graphical schematic entry methods. Additionally, the IP Integrator feature allows block-level system design using reusable modules, thereby simplifying the development process.Vivado includes a built-in simulation environment that enables designers to verify the functional and timing behavior of digital circuits. Through the use of testbenches, the functionality of the design can be validated before synthesis. The waveform viewer provides a graphical representation of signal transitions over time, which helps in analyzing circuit behavior. Debugging tools further assist in identifying and correcting design errors. These features reduce development time and improve the reliability of the final design.

The synthesis tool in Vivado converts hardware description language code into an optimized gate-level representation. During this process, the design is analyzed and optimized for area, speed, and power consumption. Vivado generates detailed synthesis reports that provide information about resource utilization and timing performance. Following synthesis, the implementation stage maps the design onto the target FPGA device. This process includes placement of logic components and routing of interconnections. The implementation tool also performs timing-driven optimization to ensure that the design meets performance requirements.

Another important feature of Vivado is the IP Integrator, which allows designers to create system-level designs using pre-built intellectual property cores. These IP blocks can be customized according to application requirements and integrated into the larger system. This feature significantly reduces design complexity and development time. Vivado also provides design rule checking, timing analysis, and power estimation tools that help improve design accuracy and performance. Timing analysis ensures that setup and hold time constraints are satisfied, while design rule checking identifies potential issues early in the design cycle.

The general design flow in Vivado begins with project creation, where the target device is selected. The next step involves design entry using hardware description languages or schematic methods. Functional simulation is then performed to verify the correctness of the design. After verification, synthesis is carried out to optimize the circuit. The implementation stage follows, where placement and routing are completed. Finally, debugging and analysis tools are used to evaluate the performance and correct any remaining issues. This structured workflow enables efficient development of high-speed digital circuits.

Vivado provides several advantages for designers and organizations. It improves productivity by offering an integrated development environment with advanced debugging tools. The synthesis and implementation engines optimize designs for better performance, reduced power consumption, and efficient resource utilization. These features help reduce design iterations and shorten development time. For organizations, Vivado enables faster time-to-market, improved product quality, and reduced development cost. The tool is supported by extensive documentation, tutorials, and community resources, which help users learn and apply advanced features effectively.Xilinx Vivado is widely used in various application domains such as digital signal processing, communication systems, embedded systems, and high-speed computing. It is also employed in emerging areas such as artificial intelligence and machine learning hardware acceleration. Due to its flexibility and powerful analysis capabilities, Vivado is well suited for designing and evaluating the MCML-based frequency divider proposed in this project. The software allows accurate simulation and performance evaluation, ensuring that the design meets the required speed and efficiency specifications.

DESIGN OF FREQUENCY DIVIDER USING MCML

This chapter presents the design methodology of the frequency divider using MOS Current Mode Logic (MCML). It describes the existing system, proposed system, block diagram, and implementation methodology. Frequency dividers are essential components in communication systems, particularly in phase-locked loops (PLLs), clock generation circuits, and frequency synthesizers. The proposed design focuses on achieving high-speed operation, reduced noise, and improved scalability using MCML-based differential logic.

Existing System

Frequency dividers are widely used in high-speed digital circuits where precise frequency scaling is required. The primary function of a frequency divider is to generate an output signal whose frequency is a fraction of the input signal. In conventional high-speed applications, MCML logic is commonly employed because of its differential operation, low voltage swing, and improved noise immunity. MCML circuits operate using a constant current source that is steered through differential transistor pairs. Unlike static CMOS circuits, which consume dynamic power during switching transitions, MCML circuits draw constant current and therefore exhibit predictable power consumption. This property enables MCML circuits to operate efficiently at very high frequencies with reduced voltage headroom.

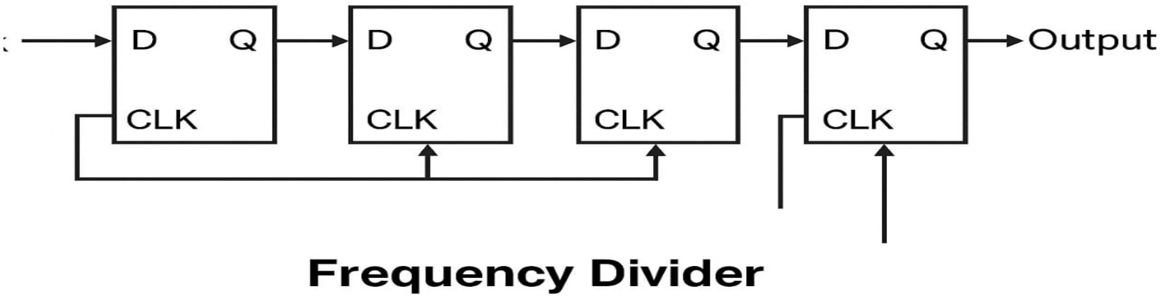


Figure 3: FREQUENCY DIVIDER

A typical MCML frequency divider is implemented using D-latches configured as toggle flip-flops. Each latch consists of a differential pair input stage, load resistors or active loads, and a constant tail current source. These latches are clocked in such a way that the output toggles at every clock cycle, thereby dividing the frequency by two. Multiple stages can be cascaded to achieve division ratios that are powers of two. The performance of the frequency divider largely depends on the design of these MCML latches. Differential pairs provide low input impedance and high-speed switching, while the bias current determines the switching speed and voltage swing. The load configuration influences the gain and delay characteristics of the circuit. Active loads using current mirrors are sometimes used to improve gain and linearity.

Differential signaling in MCML enhances common-mode noise rejection, which is beneficial in mixed-signal and RF environments. Existing designs are often optimized to minimize phase noise and jitter, especially in PLL applications. Symmetric layout techniques are employed to maintain signal integrity at high frequencies. Reduced voltage swing in MCML circuits also minimizes electromagnetic interference, making them suitable for RF systems. However, constant current operation results in higher static power consumption, which is a limitation in power-sensitive applications. To address this issue, techniques such as low-voltage MCML and adaptive biasing have been explored.

The architecture of a conventional MCML frequency divider generally consists of cascaded D flip-flops arranged in a binary counter configuration. Each stage divides the input frequency by two. As the signal propagates through successive stages, the frequency is progressively reduced. For example, in a four-stage divider, the final output frequency becomes one-sixteenth of the input clock frequency. Such structures are widely used in clock generation circuits, counters, and timing applications requiring stable low-frequency signals derived from high-frequency sources.

Proposed System

The proposed MCML-based frequency divider is designed to enhance speed, reduce power consumption, and improve scalability for high-frequency applications. The design utilizes optimized differential D flip-flops implemented using MCML topology. Unlike conventional CMOS logic, MCML maintains constant current flow and reduces voltage swing, enabling faster switching and improved noise immunity. To reduce the drawback of static power consumption, the proposed design incorporates adaptive biasing techniques that adjust current levels based on operating conditions. This approach minimizes unnecessary power dissipation while maintaining high-speed performance.

The proposed architecture consists of an input buffer, divider core, and output buffer. The input buffer conditions the incoming signal and ensures proper amplitude and impedance matching. The divider core is implemented using cascaded MCML-based divide-by-two flip-flops. Each flip-flop toggles its output on every clock cycle, thereby halving the input frequency. Additional stages can be added to achieve higher division ratios. The output buffer strengthens the divided signal and isolates the divider core from external loading effects.Careful design considerations are applied to minimize clock skew and jitter. Symmetric routing and matched differential transistor pairs are used to ensure balanced operation. Layout techniques such as common-centroid placement, guard rings, and matched load configurations improve robustness against process variations and substrate noise. The proposed design supports high-frequency operation and can be implemented in scaled CMOS technologies. Adaptive biasing reduces static power consumption while maintaining stable switching characteristics.The modular structure of the proposed divider allows flexible scaling depending on the required divide ratio. The circuit is suitable for use in PLL feedback loops, clock recovery circuits, and serializer-deserializer interfaces. Simulation results demonstrate improved switching speed, reduced jitter, and enhanced signal integrity. The proposed design maintains stable operation across process, voltage, and temperature variations, making it suitable for high-performance communication systems.

Block Diagram

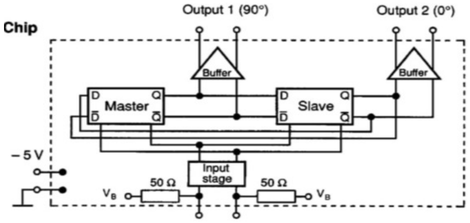


Figure 4: Block Diagram of Frequency Divider

The block diagram of the proposed MCML frequency divider consists of an input stage, master–slave flip-flop configuration, and output buffers. The input stage receives the clock signal and provides impedance matching. The master–slave configuration is implemented using MCML differential pairs to achieve divide-by-two operation. Buffers are included at the output to drive subsequent stages and maintain signal integrity. The differential outputs provide phase-shifted signals that can be used in communication and clocking applications. A constant bias supply is used to ensure steady current operation for high-speed switching.

Methodology

The design methodology follows a systematic approach to ensure proper operation of the MCML frequency divider. Initially, design specifications such as input frequency range, output frequency requirement, and allowable power consumption are defined. Based on these requirements, an appropriate MCML topology is selected. The next step involves designing basic MCML logic gates, including inverters and latches, with optimized transistor sizing and bias current levels. These gates are then used to implement the divider core by cascading divide-by-two stages.

Input and output buffers are added to improve signal conditioning and driving capability. The complete circuit is then simulated to verify functionality and evaluate performance metrics such as delay, frequency response, and power consumption. Optimization techniques are applied to improve speed and reduce power usage. After simulation, layout design is carried out with careful transistor matching and routing to minimize parasitic effects. Finally, the layout is verified to ensure correct operation and robustness under different operating conditions.

Working

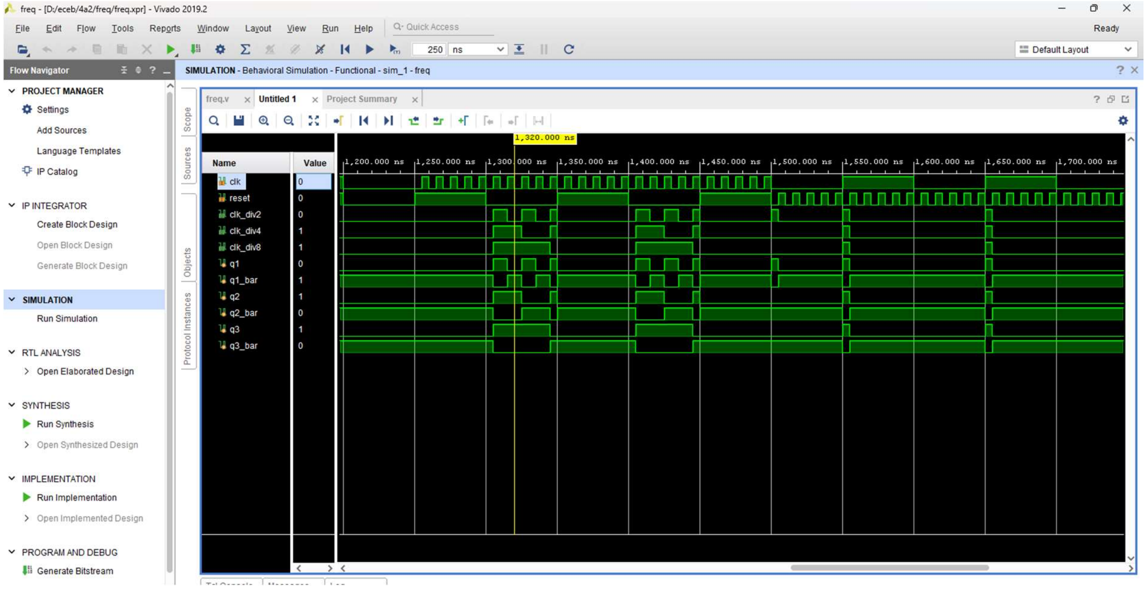
The MCML-based frequency divider is designed to operate at high frequencies while maintaining reduced power consumption and improved noise immunity. Unlike conventional CMOS logic circuits, MCML circuits rely on differential signaling and constant bias current steering, which enables faster switching and stable operation in gigahertz-range applications.

The core building block of the proposed divider consists of differential pairs of MOS transistors that steer a constant current between two output branches depending on the input logic level. This current-steering mechanism eliminates large voltage swings and reduces dynamic power consumption. As a result, MCML circuits exhibit improved performance in high-speed environments.

In the proposed design, D-latches are arranged in a toggle configuration to realize frequency division. These latches are implemented using MCML logic gates and driven by a differential clock signal. A master–slave architecture is employed to ensure correct timing and avoid race conditions. When the input clock toggles, the latch output changes state once for every two clock cycles, thereby dividing the input frequency by a factor of two.

Higher division ratios can be obtained by cascading multiple MCML latch stages. Each additional stage further divides the output frequency while preserving signal integrity. Since MCML circuits operate with constant current and limited voltage swing, they generate minimal supply noise and offer improved immunity to switching disturbances. These characteristics make MCML frequency dividers suitable for high-speed systems such as phase-locked loops, clock recovery circuits, and RF synthesizers.

Results



Name	Value
clk	0
reset	0
clk_div2	0
clk_div4	1
clk_div8	1
q1	0
q1_bar	1
q2	1
q2_bar	0
q3	1
q3_bar	0

Fig 5 :Result of Frequency divider using mcml

The simulation results confirm that the MCML frequency divider performs accurate frequency division with stable output waveforms. The output signal frequency is precisely half of the input clock frequency, demonstrating correct divide-by-two functionality.

Due to differential signaling and constant current operation, the output waveform exhibits clean transitions with reduced jitter. The smaller voltage swing inherent to MCML logic contributes to lower dynamic power consumption when compared with traditional CMOS-based dividers. This characteristic is particularly beneficial for high-speed and low-power VLSI applications.

Furthermore, the proposed design achieves fast switching speeds and reduced propagation delay, enabling operation at gigahertz frequencies. The constant current structure also improves noise immunity and minimizes supply voltage fluctuations. These features collectively enhance signal integrity and ensure reliable performance.

Overall, the simulation results validate that the MCML-based frequency divider provides precise frequency division with improved speed, reduced power consumption, and high signal quality. The design is therefore well suited for advanced communication and clock generation systems.

Conclusion

This work presented the design and implementation of a high-speed frequency divider using MOS Current Mode Logic (MCML). The MCML approach was selected due to its inherent advantages, including reduced voltage swing, constant current operation, and improved switching speed compared to conventional CMOS logic. The proposed divider was implemented using differential MCML latches arranged in a toggle configuration to achieve frequency division.

Simulation results verified that the circuit operates reliably at gigahertz-range input frequencies while maintaining low power consumption. The design demonstrated low propagation delay, reduced jitter, and improved signal integrity. Additionally, the constant current architecture minimizes supply noise and enhances stability under varying operating conditions.

The overall performance indicates that the MCML-based frequency divider is suitable for high-speed VLSI applications such as phase-locked loops, frequency synthesizers, and clock recovery systems. The study also highlighted that folded and complementary MCML structures can further enhance performance at lower supply voltages.

Future Scope

The proposed MCML frequency divider can be extended in several directions to enhance performance and broaden its applications. One possible improvement is technology scaling to deep submicron nodes such as 28 nm and 14 nm. This scaling can further increase operating speed while reducing power consumption, making the design suitable for modern high-frequency communication systems.

Future work may also focus on integrating the MCML divider into complete systems such as phase-locked loops, RF synthesizers, and clock generation modules. The development of programmable or multi-modulus frequency dividers can improve flexibility and enable use in reconfigurable communication architectures.

Another important extension is robustness analysis under process, voltage, and temperature variations. Evaluating the design under PVT conditions ensures reliable performance across different operating environments. Hybrid architectures combining MCML and CMOS logic may also be explored to optimize power consumption, chip area, and performance simultaneously.

Finally, implementing physical layout, performing post-layout simulations, and fabricating the design in silicon will validate the proposed architecture in real-world conditions. Such work can pave the way for practical deployment in high-speed VLSI and RF integrated circuits.

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